SEARCH REQUEST FORM **Scientific and Technical Information Center - EIC2800**

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Date 8/7/02 Serial # 09/805,027 Priority Application Date 3/12/01

Your Name M. Lewis Examiner # _____

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In what format would you like your results? Paper is the default. PAPER DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case? 08-07-02 P05:11 OUT

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ___ Nonpatent Literature ___ Other _____

Secondary Refs ✓ Foreign Patents ___

Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-10

Problem: Page 2 Lines 9-32
" 3 " 1-32
" 4 " 1-32
" 5 " 1-5

Solution: " 6 " 1-17

Staff Use Only	Type of Search	Vendors
Searcher: I. Speckard	Structure (#)	STN ✓
Searcher Phone: 308-6559	Bibliographic ✓	Dialog ✓
Searcher Location: STIC-EIC2800, CP4-9C18	Litigation	Questel/Orbit
Date Searcher Picked Up: 8/9/02	Fulltext ✓	Lexis-Nexis
Date Completed: 8/9/02	Patent Family	WWW/Internet
Searcher Prep/Rev Time: 70	Other	Other
Online Time: 140		

(FILE 'HOME' ENTERED AT 13:27:40 ON 09 AUG 2002)

FILE 'REGISTRY' ENTERED AT 13:28:02 ON 09 AUG 2002

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                E COPPER/CN
L1              1 SEA ABB=ON  PLU=ON  COPPER/CN
                E ALUMINUM/CN
L2              1 SEA ABB=ON  PLU=ON  ALUMINUM/CN
                E ALUMINIUM/CN
L3              1 SEA ABB=ON  PLU=ON  ALUMINIUM/CN
                E TANTALUM/CN
L4              1 SEA ABB=ON  PLU=ON  TANTALUM/CN
                E NITRIDE/CN
L5              1 SEA ABB=ON  PLU=ON  NITRIDE/CN
                E TITANIUM/CN
L6              1 SEA ABB=ON  PLU=ON  TITANIUM/CN
                E SILANE/CN
L7              1 SEA ABB=ON  PLU=ON  SILANE/CN
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FILE 'CAPLUS' ENTERED AT 13:34:33 ON 09 AUG 2002

FILE 'REGISTRY' ENTERED AT 13:35:18 ON 09 AUG 2002

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L8              6 SEA ABB=ON  PLU=ON  (L1 OR L2 OR L3 OR L4 OR L5 OR L6 OR L7)
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FILE 'CAPLUS' ENTERED AT 13:35:35 ON 09 AUG 2002

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L9        1734673 SEA ABB=ON  PLU=ON  COPPER OR CUALUMINUM OR ALUMINIUM OR AL OR
                  (TANTALUM OR TA)(W)(NITRIDE OR N) OR (TITANIUM OR TI)(W)(NITRID
                  E OR N) OR SILANE OR L8
L10        157438 SEA ABB=ON  PLU=ON  (SEMICONDUCT######(1A)DEVICE)
L11         68670 SEA ABB=ON  PLU=ON  (INTEGRAT######(3A)CIRCUIT) OR IC
L12           526 SEA ABB=ON  PLU=ON  INTEGRAT#######(3A)DENSIT#######
L13          8210 SEA ABB=ON  PLU=ON  PLASMA(3A)OXIDE
L14        116903 SEA ABB=ON  PLU=ON  PVD OR (PLASMA(W)VAPOR(W)DEPOSIT######) OR
                  (VAPOR(W)DEPOSIT######)
L15         23454 SEA ABB=ON  PLU=ON  STUD######(3A)(CONNECTION OR BRACE OR LINK
                  OR CHAIN)
L16         13853 SEA ABB=ON  PLU=ON  LINER
L17            13 SEA ABB=ON  PLU=ON  (ELIMINAT####### OR MINIMIZ####### OR
                  MINIMIS#####)(3A)((METAL########(3A)MIGRAT#########))
L18         14212 SEA ABB=ON  PLU=ON  L9 AND (L11 OR L12)
L19        412732 SEA ABB=ON  PLU=ON  SEMICONDUCT##########
L20        412732 SEA ABB=ON  PLU=ON  (L10 OR L19)
L21         69051 SEA ABB=ON  PLU=ON  (L11 OR L12)
L22          5295 SEA ABB=ON  PLU=ON  L18 AND L20
L23            56 SEA ABB=ON  PLU=ON  L22 AND L13
L24            30 SEA ABB=ON  PLU=ON  L23 AND L14
L25             0 SEA ABB=ON  PLU=ON  L24 AND L15
L26             2 SEA ABB=ON  PLU=ON  L24 AND L16
L27             4 SEA ABB=ON  PLU=ON  L9 AND L17
                D BIB 1-4
L28         68761 SEA ABB=ON  PLU=ON  L9 AND L20
L29          6786 SEA ABB=ON  PLU=ON  L28 AND L14
L30           200 SEA ABB=ON  PLU=ON  L29 AND L13
L31             0 SEA ABB=ON  PLU=ON  L30 AND (METAL########(3A)MIGRAT#########)
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L32            0 SEA ABB=ON  PLU=ON  L30 AND L15
L33            0 SEA ABB=ON  PLU=ON  L30 AND ((CIRCUIT OR IC)(3A)CHIP)
L*** DEL       0 S L30 AND S11
L34           29 SEA ABB=ON  PLU=ON  L30 AND L11
L35           29 DUP REM L34 (0 DUPLICATES REMOVED)
L36           29 SEA L35
L40            0 SEA ABB=ON  PLU=ON  L39 AND (PITCH###(3A)INTERLEVEL)
L41           29 SEA L35
L42            1 SEA ABB=ON  PLU=ON  L41 AND INTERLEVEL
L43           28 SEA ABB=ON  PLU=ON  L41 NOT L42
L44            2 SEA ABB=ON  PLU=ON  L43 AND (INTERLAYER OR INTER(W)LAYER)
L45           26 SEA ABB=ON  PLU=ON  L43 NOT L44
L46            1 SEA ABB=ON  PLU=ON  L45 AND (INTERCONNECT OR INTER(W)CONNECT
L47           25 SEA ABB=ON  PLU=ON  L45 NOT L46
L48            2 SEA ABB=ON  PLU=ON  L47 AND STUD####
L49           23 SEA ABB=ON  PLU=ON  L47 NOT L48
L50            0 SEA ABB=ON  PLU=ON  L49 AND (VIA(3A)LINER)
                 D S49 BIB AB ALL
L51           23 SEA ABB=ON  PLU=ON  L47 NOT L48
```

L26 ANSWER 1 OF 2 CAPLUS COPYRIGHT 2002 ACS
AN 2001:668332 CAPLUS
DN 135:219711
TI CVD plasma assisted low dielectric constant films
IN Cheung, David; Yau, Wai-fan; Mandal, Robert R.
PA Applied Materials, Inc., USA
SO U.S., 22 pp., Cont.-in-part of U.S. 6,072,227.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 8

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6287990	B1	20010911	US 1998-162915	19980929
	US 6054379	A	20000425	US 1998-21788	19980211
	US 2001004479	A1	20010621	US 1998-185555	19981104
	US 6303523	B2	20011016		
	WO 9941423	A2	19990819	WO 1999-US2903	19990210
	WO 9941423	A3	19991028		
	W: JP, KR, SG				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	TW 408369	B	20001011	TW 1999-88102101	19990210
	EP 1055012	A2	20001129	EP 1999-906897	19990210
	R: BE, DE, GB, NL				
	JP 2002503879	T2	20020205	JP 2000-531599	19990210
	US 6348725	B1	20020219	US 1999-247381	19990210
	US 6340435	B1	20020122	US 1999-329012	19990609
	US 2002000670	A1	20020103	US 1999-477126	19991230
	US 2002045361	A1	20020418	US 2001-957551	20010919
	US 2002084257	A1	20020704	US 2001-11369	20011105
PRAI	US 1998-21788	A2	19980211		
	US 1998-114682	A2	19980713		
	US 1998-162915	A2	19980929		
	US 1998-185555	A	19981104		
	US 1998-189555	B2	19981111		
	US 1999-247381	A1	19990210		
	WO 1999-US2903	W	19990210		
	US 1999-329012	A1	19990609		

AB A method and app. for depositing a low dielec. const. film by reaction of an organosilane or organosiloxane compd. and an oxidizing gas at a low RF power level from 10-250 W. The oxidized organosilane or organosiloxane film has good barrier properties for use as a **liner** or cap layer adjacent other dielec. layers. The oxidized organosilane or organosiloxane film may also be used as an etch stop or an intermetal dielec. layer for fabricating dual damascene structures. The oxidized organosilane or organosiloxane films also provide excellent adhesion between different dielec. layers. A preferred oxidized organosilane film is produced by reaction of methylsilane (MeSiH3), or dimethylsilane (Me2SiH2), and nitrous oxide (N2O), at an RF power level from .apprx.10 to 200 W or a pulsed RF power level from .apprx.20 to 250 W during 10-30 of the duty cycle.
RE.CNT 123 THERE ARE 123 CITED REFERENCES AVAILABLE FOR THIS RECORD

ALL CITATIONS AVAILABLE IN THE RE FORMAT

L26 ANSWER 2 OF 2 CAPLUS COPYRIGHT 2002 ACS
AN 1998:250681 CAPLUS
DN 128:303026
TI Shallow trench isolation (STI) method employing gap filling silicon oxide dielectric layer
IN Jang, Syun-ming; Chen, Ying-ho; Yu, Chen-hua
PA Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5741740	A	19980421	US 1997-873836	19970612

AB There is 1st provided a Si substrate having a trench formed in it. The Si substrate is thermally oxidized to form a thermal Si oxide trench **liner** layer within the trench. A conformal Si oxide intermediate layer is formed on the thermal Si **oxide** trench **liner** by **plasma**-enhanced CVD method employing a **silane** Si source material. Finally, a gap-filling Si oxide trench fill layer is formed on the conformal Si oxide intermediate layer by sub-atm.-pressure thermal CVD employing O3 and TEOS. To provide improved properties of the gap-filling Si oxide trench fill layer, the thermal Si oxide trench **liner** layer may be treated with a N-contg. plasma prior to forming the conformal Si oxide intermediate layer.

L27 ANSWER 1 OF 4 CAPLUS COPYRIGHT 2002 ACS
AN 2001:185253 CAPLUS
DN 134:201644
TI **Al** interconnection of semiconductor integrated circuit devices
IN Terajima, Hidenobu
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001068473	A2	20010316	JP 1999-236664	19990824

AB The invention relates to a semiconductor integrated circuit device having **Al** interconnections, wherein the electromigration and stress **migration** of refractory **metal** component are **minimizes** by optimized circuit layout.

L27 ANSWER 2 OF 4 CAPLUS COPYRIGHT 2002 ACS
AN 1999:789859 CAPLUS
DN 132:29579
TI Ceramic electronic components having electrodes connected to lead wires by soldering and ceramic electronic devices using thereof
IN Nagao, Yoshitaka; Hirota, Toshiharu; Kawahara, Takahiko; Namikawa, Yasunori; Abe, Yoshiaki; Okamoto, Tetsukazu
PA Murata Mfg. Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11345704	A2	19991214	JP 1998-152758	19980602

AB The title electrodes are triple layer laminates comprising (1) a lower layer made from **Al**, Ti, Cr, Ni, and/or Zn for ohmic contacting to the ceramic substrate, (2) an intermediate layer made from Ni or a Ni alloy for heat resistance, and (3) an upper layer made from Cu or Au for migration resistance. The triple layer electrode having a Cu or Au upper layer provided in elec. components such as thermistors prevents **metal migration** and consequently **eliminates** discharge or short circuiting between the electrodes.

L27 ANSWER 3 OF 4 CAPLUS COPYRIGHT 2002 ACS
AN 1982:448048 CAPLUS
DN 97:48048
TI A lithium tantalate (LiTaO3) SAW resonator and its application to video cassette recorder
AU Ebata, Yasuo; Sato, Koji; Morishita, Shigefumi
CS Toshiba Res. Dev. Cent., Kawasaki, 210, Japan
SO Ultrason. Symp. Proc. (1981), 1, 111-16
CODEN: ULSPDT; ISSN: 0090-5607
DT Journal
LA English
AB The driving-power limitation of LiTaO3 SAW (surface-acoustic-wave) resonators for use as radio-frequency converters in video cassette recorders was extended by >50 times by adding 0.3-1.0 wt.% Cu to the **Al** metalization to **eliminate** stress-induced **metal migration**.

L27 ANSWER 4 OF 4 CAPLUS COPYRIGHT 2002 ACS
AN 1980:225322 CAPLUS
DN 92:225322
TI Semiconductor device production
IN Lien, Suei-Yuen P.
PA Western Electric Co., Inc., USA
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 4190467	A	19800226	US 1978-970031	19781215
	WO 8001333	A1	19800626	WO 1979-US1017	19791126
	W: DE, GB, JP				
	JP 56500233	T2	19810226	JP 1980-500264	19791126
	JP 59046090	B4	19841110		
	GB 2057759	A	19810401	GB 1980-25378	19791126
	GB 2057759	B2	19830126		
	GB 2057759	A1	19810401		
	DE 2953410	C2	19850131	DE 1979-2953410	19791126
	DE 2953410	T	19810108		
	FR 2444338	A1	19800711	FR 1979-30321	19791211
	FR 2444338	B1	19850322		
PRAI	US 1978-970031		19781215		
	WO 1979-US1017		19791126		

AB A thermal-gradient zone melting method is described for **eliminating** distortion of the **migrated metal** pattern by including a peripheral ring of the metal adjacent to the edge of the semiconductor wafer. Thus, thermal migration of **Al** through an n-type (111) Si wafer (10-20 .OMEGA.-cm) 10 mils thick was performed. A grid pattern of 40 .times. 40 mils with 6-mil line width was generated on the 1st surface of the wafer by conventional methods followed by thermal migration at 1220.degree. with an estd. temp. gradient of 50-100.degree./cm. The grid pattern included a ring of **Al** on the outer periphery of the wafer. Thermal migration was continued until the grid pattern had migrated completely through the wafer to the opposite surface. The resulting wafer showed no substantial distortion of the grid pattern and all grid lines extended to the edge of the wafer.

L42 ANSWER 1 OF 1 CAPLUS COPYRIGHT 2002 ACS
AN 2000:680413 CAPLUS
DN 133:246186
TI Fabrication of a scalable and reliable **integrated circuit** inter-level dielectric
IN Sahota, Kashmir; Huang, Richard J.; Chen, Hung-Sheng; Sun, Yu
PA Advanced Micro Devices, Inc., USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6124640	A	20000926	US 1998-144506	19980831

AB An inter-level dielec. (ILD) is formed from a lower barrier layer comprising a conformal Si oxynitride layer, a gap fill layer comprising a high-d. **plasma** (HDP) **oxide** and a cap layer. The use of HDP oxide as a gap fill layer enables better control of the ILD thickness, avoids outgassing problems, facilitates via formation and reduces planarization.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L44 ANSWER 1 OF 2 CAPLUS COPYRIGHT 2002 ACS
AN 2000:383819 CAPLUS
DN 133:11760
TI Plasma deposition of an **interlayer** insulating film for flat covering a wiring layer of an **integrated circuit**
IN Tokumasu, Noboru; Maeda, Kazuo
PA Canon Sales Co., Inc., Japan; Semiconductor Process Laboratory Co., Ltd.
SO Eur. Pat. Appl., 29 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1006569	A2	20000607	EP 1999-114234	19990727
	EP 1006569	A3	20010718		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 2000174013	A2	20000623	JP 1998-345404	19981204
	JP 3251554	B2	20020128		
	US 6221755	B1	20010424	US 1999-358399	19990722
	TW 413850	B	20001201	TW 1999-88112529	19990723
	KR 2000047452	A	20000725	KR 1999-31795	19990803
PRAI	JP 1998-345404	A	19981204		

AB Disclosed is a film formation method of an **interlayer** insulating film which is flattened to cover a wiring layer of a **semiconductor integrated circuit** device, in which a film-forming gas is activated by converting the film-forming gas into a plasma, the film-forming gas being composed of either a mixed gas contg. a P-contg. compd. contg. trivalent P, which takes a Si-O-P structure, and a Si-contg. compd. contg. at most one O atom or an addnl. mixed gas prepd. by adding an oxidative gas to said mixed gas; and a Si-contg. insulating film contg. P2O5 is formed on a substrate.

L44 ANSWER 2 OF 2 CAPLUS COPYRIGHT 2002 ACS
AN 1999:653379 CAPLUS
DN 131:265760
TI **Semiconductor devices** and methods for their fabrication
IN Koo, Bon Jae
PA Samsung Electronics Co. Ltd., S. Korea
SO Ger. Offen., 12 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 19860829	A1	19991007	DE 1998-19860829	19981230
	TW 388989	B	20000501	TW 1998-87118834	19981113
	FR 2776833	A1	19991001	FR 1999-2959	19990310
	JP 11330390	A2	19991130	JP 1999-74491	19990318
	CN 1230779	A	19991006	CN 1999-103428	19990330
	US 2001023080	A1	20010920	US 1999-281706	19990330
PRAI	KR 1998-10989	A	19980330		

AB An improved **semiconductor device** and fabrication method thereof, without a deterioration of the properties of a ferroelec. capacitor normally caused by a covering dielec. **interlayer**. The new fabrication method is devised in such a way that a tensile stress exists between the dielec. **interlayer** and the capacitor. The dielec. **interlayer** can be a low temp. oxide layer as, for example, a plasma-enhanced-TEOS, undoped silicate glass(USG) or electron-cyclotron resonance-produced silicon oxide.

L46 ANSWER 1 OF 1 CAPLUS COPYRIGHT 2002 ACS
AN 2002:271968 CAPLUS
DN 136:287764
TI Combined gate cap or digit line and spacer deposition using high d. **plasma** CVD of silicon **oxide** or silicon nitride
IN Li, Weimin; Sharan, Sujit; Sandhu, Gurtej
PA Micron Technology, Inc., USA
SO U.S., 17 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6368988	B1	20020409	US 1999-354572	19990716
	US 2002076947	A1	20020620	US 2001-989036	20011121
PRAI	US 1999-354572	A3	19990716		

AB A method for fabricating gate electrodes and gate **interconnects** with a protective Si oxide or Si nitride cap and spacer formed by high d. plasma CVD (HDPCVD). Si oxide or Si nitride is deposited in a reaction zone of a HDPCVD reactor while providing .gtoreq.2 selected substrate bias powers, source powers and/or selected gas mixts. to tailor the shape and thickness of the film for desired applications. A low bias power of below 500 W is provided in a 1st stage HDPCVD and the bias power is then increased to at 500-3000 W for a 2nd stage to produce a protective film having thin sidewall spacers for enhanced **semiconductor device** d. and a relatively thick cap.
RE.CNT 33 THERE ARE 33 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L48 ANSWER 2 OF 2 CAPLUS COPYRIGHT 2002 ACS
AN 1998:60769 CAPLUS
DN 128:187064
TI Ultrathin oxide gate dielectrics prepared by low temperature remote plasma-assisted oxidation
AU Niimi, H.; Lucovsky, G.
CS Computer Engineering, Electrical, Physics, Departments of Materials Science and Engineering, North Carolina State University, Raleigh, NC, 27695-8202, USA
SO Surface and Coatings Technology (1998), 98(1-3), 1529-1533
CODEN: SCTEEJ; ISSN: 0257-8972
PB Elsevier Science S.A.
DT Journal
LA English
AB Monolayer N-atom incorporation at Si-SiO2 interfaces in device-quality SiO2 gate oxides has been accomplished by a three-step low-thermal budget process: (i) 300.degree.C remote plasma-assisted oxidn. in N2O to form the nitrided Si-SiO2 interface, (ii) 300.degree.C remote plasma-assisted chem. **vapor deposition** from SiH4 and O2 or N2O to form the oxide layer, and (iii) a 30 s 900.degree.C post-deposition rapid thermal anneal for chem. and structural relaxation. This paper reports on an extension of low-temp. plasma processing to ultra-thin gate dielecs. (<3 nm) that is based on the first of the three steps identified above: the 300.degree.C remote plasma-assisted oxidn. in O2 or N2O. This paper: (i) highlights interrupted processing Auger electron spectroscopy measurements to monitor (a) growth rate and (b) interfacial nitrogen; (ii) discusses the reactions pathways for the **plasma**-assisted **oxide** growth process; (iii) contrasts (a) plasma-assisted and (b) furnace and rapid thermal oxidn. processes.

L51 ANSWER 1 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 2002:534018 CAPLUS
DN 137:102415
TI Process for inhibiting crack formation in low dielectric constant dielectric films of **integrated circuit** structure
IN Catabay, Wilbur G.; Hsia, Wei-jen; Qiang, Hong
PA LSI Logic Corporation, USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6420277	B1	20020716	US 2000-704635	20001101

AB A process is disclosed which inhibits cracking of the layer of low k Si oxide dielec. material on an **integrated circuit** structure during subsequent processing of the layer of low k Si oxide dielec. material. The process comprises: forming a layer of low k Si oxide dielec. material on an **integrated circuit** structure on a **semiconductor** substrate, and forming over the layer of low k Si oxide dielec. material a capping layer of dielec. material having: a dielec. const. not exceeding .apprx.4, a thickness of at least .apprx.300 nm, and a compressive stress of at least .apprx.3 .times. 109 dynes/cm2. In a preferred embodiment, the capping layer comprises Si oxide formed by reaction of **silane** and N2O in a PECVD process carried out within a pressure range of from .apprx.600 to .apprx.1000 mTorr; and a temp. range of from .apprx.300 to .apprx.400.degree.; while maintaining a plasma at a power level ranging from .apprx.250 to .apprx.350 W; a flow of **silane** equiv. to a flow of from .apprx.35 sccm to .apprx.45 sccm into a 10 L reactor; and a flow of N2O equiv. to a flow of from .apprx.3800 sccm to .apprx.4200 sccm into the 10 L reactor.

RE.CNT 55 THERE ARE 55 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L51 ANSWER 2 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 2002:425392 CAPLUS
DN 136:410116
TI Method of improved **copper** gap fill
IN Chen, Sheng-hsiung; Tsai, Ming-hsing
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6399486	B1	20020604	US 1999-442313	19991122

AB The invention relates to an annealing process to "heal" electrochem. **copper** deposited (ECD) defects in a dual damascene via and trench structure. The annealing step is processed after the electrochem. deposition (ECD) of the top excess **copper** and before the chem. mech. polishing (CMP) of the **copper**. The key processing steps of this invention are the special annealing steps at key temps., ambient, pressures and times to anneal out the defective **copper** voids in the dual damascene structure. These annealing conditions are special annealing steps to promote low temp. **copper** surface diffusion to "heal" the voids and other defectives within the **copper** trench and via structure. The special annealing conditions of: temp., ambient, pressure and time are the following: temp. in a range of about 300 to 500.degree., ambient of nitrogen N2, hydrogen H2 gases (reducing atm. to remove **copper oxide**, N2/H2 **plasma** preferred), pressure in a range of about 100 MPa to 600 MPa, time in a range of about 0.5 to 10 min. These conditions are designed to take advantage of low temp. surface diffusion mechanisms.

RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L51 ANSWER 3 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 2002:256791 CAPLUS
DN 136:287681
TI Method of manufacturing a **semiconductor integrated circuit** device with high aspect ratio hole or trench
IN Ikeda, Takenobu; Tadokoro, Masahiro; Izawa, Masaru; Yunogami, Takashi
PA Japan
SO U.S. Pat. Appl. Publ., 59 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002039843	A1	20020404	US 2001-964628	20010928
	JP 2002110647	A2	20020412	JP 2000-299854	20000929
PRAI	JP 2000-299854	A	20000929		

AB A hole is formed on an insulating film made of Si **oxide** by selectively **plasma**-etching the insulating film with an etching gas contg. C5F8, O2, and Ar firstly under a condition in which the deposition property of a polymer layer is weak and secondly under a condition in which that of the polymer layer is strong.

L51 ANSWER 4 OF 23 CAPLUS . COPYRIGHT 2002 ACS
AN 2001:933102 CAPLUS
DN 136:46734
TI Plasma treatment for decreasing the microporosity induced by stress corrosion in etched metal conductor-line patterns
IN Ngo, Minh Van; Chan, Simon S.; Sanderfer, Anne E.; Ko, King Wai Kelwin
PA Advanced Micro Devices, Inc., USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6333263	B1	20011225	US 1999-285388	19990402
	US 2001007791	A1	20010712	US 2001-765426	20010122
PRAI	US 1999-285388	A1	19990402		

AB The micropores induced by stress corrosion in etched pattern of metal conductor lines are prevented by: (a) wet cleaning of the patterned metal lines with a solvent, to remove the etching residues; and (b) final pattern treatment with N2-contg. plasma, typically for 20-70 s at .gtoreq.400.degree.; and (c) filling the line-pattern gaps with a dielec., esp. by chem. **vapor deposition** of **oxide** from high-d. **plasma**. The process is suitable for applying the **Al**, **Al**-alloy, and other metal conductor lines with a close spacing and multiple layers on **semiconductor** wafers.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L51 ANSWER 5 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 2001:668332 CAPLUS
DN 135:219711
TI CVD plasma assisted low dielectric constant films
IN Cheung, David; Yau, Wai-fan; Mandal, Robert R.
PA Applied Materials, Inc., USA
SO U.S., 22 pp., Cont.-in-part of U.S. 6,072,227.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 8

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6287990	B1	20010911	US 1998-162915	19980929
	US 6054379	A	20000425	US 1998-21788	19980211
	US 2001004479	A1	20010621	US 1998-185555	19981104
	US 6303523	B2	20011016		
	WO 9941423	A2	19990819	WO 1999-US2903	19990210
	WO 9941423	A3	19991028		
	W: JP, KR, SG				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	TW 408369	B	20001011	TW 1999-88102101	19990210
	EP 1055012	A2	20001129	EP 1999-906897	19990210
	R: BE, DE, GB, NL				
	JP 2002503879	T2	20020205	JP 2000-531599	19990210
	US 6348725	B1	20020219	US 1999-247381	19990210
	US 6340435	B1	20020122	US 1999-329012	19990609
	US 2002000670	A1	20020103	US 1999-477126	19991230
	US 2002045361	A1	20020418	US 2001-957551	20010919
	US 2002084257	A1	20020704	US 2001-11369	20011105
PRAI	US 1998-21788	A2	19980211		
	US 1998-114682	A2	19980713		
	US 1998-162915	A2	19980929		
	US 1998-185555	A	19981104		
	US 1998-189555	B2	19981111		
	US 1999-247381	A1	19990210		
	WO 1999-US2903	W	19990210		
	US 1999-329012	A1	19990609		

AB A method and app. for depositing a low dielec. const. film by reaction of an organosilane or organosiloxane compd. and an oxidizing gas at a low RF power level from 10-250 W. The oxidized organosilane or organosiloxane film has good barrier properties for use as a liner or cap layer adjacent other dielec. layers. The oxidized organosilane or organosiloxane film may also be used as an etch stop or an intermetal dielec. layer for fabricating dual damascene structures. The oxidized organosilane or organosiloxane films also provide excellent adhesion between different dielec. layers. A preferred oxidized organosilane film is produced by reaction of methylsilane (MeSiH3), or dimethylsilane (Me2SiH2), and nitrous oxide (N2O), at an RF power level from .apprx.10 to 200 W or a pulsed RF power level from .apprx.20 to 250 W during 10-30 of the duty cycle.
RE.CNT 123 THERE ARE 123 CITED REFERENCES AVAILABLE FOR THIS RECORD

L51 ANSWER 6 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 2001:627221 CAPLUS
DN 135:188913
TI Plasma enhanced chemical **vapor deposition** (PECVD) method for forming microelectronic layer with enhanced film thickness uniformity
IN Wang, Ying-lang; Wang, Hui-ling; Dun, Jowei; Wu, Szu-an
PA Taiwan Semiconductor Manufacturing Co., Taiwan
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6281146	B1	20010828	US 1999-396517	19990915

AB A method is presented for forming a microelectronic layer. First, a substrate is provided. Over the substrate the microelectronic layer is formed while employing a plasma enhanced CVD (PECVD) method employing a source material gas and a carrier gas, in which there is employed a sufficiently low plasma power, a sufficiently low source material gas:carrier gas flow rate ratio and a sufficiently high carrier gas at. mass such that the microelectronic layer is formed with enhanced film thickness uniformity. The method may be employed for forming ion implant screen layers, such as Si oxide ion implant screen layers, with enhanced film thickness uniformity.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L51 ANSWER 7 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 2001:464353 CAPLUS
DN 135:54470
TI Ultrathin deposited gate dielectric formation using low-power, low-pressure PECVD for improved **semiconductor device** performance
IN Sun, Sey-Ping; Gardner, Mark I.; May, Charles E.
PA Advanced Micro Devices, Inc., USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6251800	B1	20010626	US 1999-227513	19990106

AB An ultrathin gate dielec. and a method for forming the same are provided. The gate dielec. is believed to allow enhanced performance of **semiconductor devices** including transistors and dual-gate memory cells. A low-power, low-pressure plasma-enhanced CVD (PECVD) method employing **silane** and nitrous oxide sources is used to deposit the dielec. As compared to conventional PECVD deposition, the method uses lower **silane** and nitrous oxide flow rates, a more dil. **silane** in N2 mixt., a lower chamber pressure, and a lower radio frequency power d. These settings allow plasma conditions to stabilize so that deposition may be performed in time increments at least as short as 0.1 s, so that oxide thicknesses at least as small as 1 .ANG. may be controllably deposited. The oxide is preferably deposited in portions at multiple substrate mounting positions in a deposition chamber. Combination of oxide portions in this manner is believed to reduce the d. of pinholes in the oxide, and the low-power, low-pressure deposition conditions are further believed to reduce **plasma** damage to the **oxide** and reduce the d. of trap states in the oxide. A rapid thermal anneal of the oxide may be performed after deposition, and may improve the quality of the interface between the oxide and the underlying **semiconductor** substrate.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L51 ANSWER 8 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 2001:247698 CAPLUS
DN 134:260117
TI Dual damascene flowable oxide insulation structure and metallic barrier for **semiconductor devices**
IN Greco, Stephen; Hummel, John; Liu, Joyce; Mcgahay, Vincent; Mih, Rebecca; Srivastava, Kamalesh
PA USA
SO U.S. Pat. Appl. Publ., 21 pp., Division of U.S. Ser. No. 408,351.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001000115	A1	20010405	US 2000-725862	20001130
	US 6221780	B1	20010424	US 1999-408351	19990929
PRAI	US 1999-408351	A3	19990929		

AB A method and structure for protecting a flowable oxide insulator in a **semiconductor** by oxidizing sidewalls of the FOX insulator, optionally nitriding the oxidized FOX sidewalls, and then covering all surfaces of a trough or plurality of troughs in the FOX insulator, including the sidewalls, with a conductive secondary protective layer. In a multiple layer damascene structure, the surface of the FOX insulator is also oxidized, an addnl. oxide layer is deposited thereon, and a nitride layer deposited on the oxide layer. Then steps are repeated to obtain a comparable damascene structure. The materials can vary and each damascene layer nay be either a single damascene or a dual damascene layer.

L51 ANSWER 9 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 2001:161468 CAPLUS
DN 134:187142
TI Combining CMP and wet or dry etching for fabrication of shallow trench isolation for **integrated circuits**
IN Jang, Syun-Ming; Chen, Ying-Ho
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6197660	B1	20010306	US 1999-301223	19990429

AB Shallow trench isolation in which trenches having varying dimensions were formed in a hard surface such as Si nitride can lead to dishing inside the larger trenches. To overcome this, the trenches were 1st over-filled with a layer of HDPCVD oxide followed by the deposition of a relatively soft dielec. layer, using a conformal deposition method. CMP was then used to remove both the added layer and most of the original HDPCVD oxide, a small thickness of the latter being left in place. Because of the earlier influence of the added layer the resulting surface was planar and a conventional wet or dry etch could be used to remove the remaining oxide, thereby exposing the top surface and fully filling the trenches without any dishing.
RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L51 ANSWER 10 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 2001:129947 CAPLUS
DN 134:171919
TI Deposition of an oxide layer to facilitate photoresist rework on polygate layer
IN Singh, Bhanwar; Yedur, Sanjay K.; Rangarajan, Bharath
PA Advanced Micro Devices, Inc., USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6191046	B1	20010220	US 1999-266362	19990311

AB A method of reworking a photoresist used to pattern a **semiconductor** structure is provided. A dielec. layer is formed over an anti-reflective coating, the anti-reflective coating covering a 1st underlayer, the 1st underlayer covering a 2nd underlayer. A 1st photoresist layer is formed and patterned over the dielec. layer to yield a desired photoresist pattern. An undesired feature in the patterned 1st photoresist layer is detd. The patterned 1st photoresist layer is removed. A 2nd photoresist layer is formed and patterned over the dielec. layer. Exposed portions of the dielec. layer, the anti-reflective coating and the 1st underlayer are etched. A thin photoresist layer is formed over exposed portions of the 2nd underlayer. A CMP process was performed to remove the dielec. layer. The thin photoresist layer is stripped.

RE.CNT 17 THERE ARE 17 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L51 ANSWER 11 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 2001:45140 CAPLUS
DN 134:94407
TI Silicon oxide dielectric material with excess silicon as diffusion barrier layer for **semiconductor device** fabrication
IN Bao, Tien-i; Jang, Syun-ming
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6174797	B1	20010116	US 1999-435678	19991108

AB A method for forming upon a substrate employed within a microelectronics fabrication a 1st dielec. layer, an intermediate diffusion barrier dielec. layer and a conductor layer which comprise an inter-level metal dielec. (IMD) layer with attenuated diffusion between the dielec. layers and conductor layer. There is 1st provided a substrate employed within a microelectronics fabrication. There is then formed upon the substrate a patterned microelectronics layer. There is then formed over the substrate a 1st dielec. layer. There is then formed over the substrate a diffusion barrier dielec. layer. There is then formed over the substrate a conductor layer to complete an inter-level metal dielec. (IMD) layer with attenuated inter-diffusion between the dielec. layers and conductor layer.
RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L51 ANSWER 12 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 2000:909179 CAPLUS
DN 134:64990
TI Void forming method for fabricating low dielectric constant dielectric layer
IN Jang, Syun-Ming
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6165897	A	20001226	US 1998-86823	19980529

AB A method for forming a dielec. layer within a microelectronics fabrication. There is 1st provided a microelectronics substrate layer employed within a microelectronics fabrication. There is then formed upon the microelectronics substrate layer a patterned microelectronics layer. There is then formed conformally over the patterned microelectronics layer a conformal Si oxide dielec. layer formed employing a plasma enhanced CVD (PECVD) method employing **silane** as a Si source material. The conformal Si oxide dielec. layer comprises: (1) a 1st region formed over the upper surface of the patterned microelectronics layer; (2) a 2nd region formed interposed between patterns which comprises the patterned microelectronics layer and parallel with sidewalls of patterns which comprises the patterned microelectronics layer; and (3) a 3rd region formed interposed between patterns which comprises the patterned microelectronics layer but not parallel with sidewalls of patterns which comprises the patterned microelectronics layer. There is then treated with an O contg. **plasma** the conformal Si **oxide** dielec. layer to enhance the rate of formation of a 2nd Si oxide dielec. layer upon the 1st region of the conformal Si oxide dielec. layer with respect to at least the 2nd region of the conformal Si oxide dielec. layer. The 2nd Si oxide dielec. layer is formed employing an ozone assisted thermal CVD method employing tetraethylorthosilicate (TEOS) as a Si source material. Finally, there is then formed upon the O contg. **plasma** treated conformal Si **oxide** dielec. layer the 2nd Si oxide dielec. layer, where the 2nd Si oxide dielec. layer defines, at least in part, voids formed interposed between patterns which comprises the patterned microelectronics layer.

RE.CNT 16 THERE ARE 16 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L51 ANSWER 13 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 2000:252998 CAPLUS
DN 132:259322
TI Plasma etch method for forming metal-fluoropolymer residue free vias through silicon containing dielectric layers
IN Chu, Po-Tao; Yeh, Ming-Chieh; Chen, Fang-Cheng; Lu, Ting-Yih
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6051505	A	20000418	US 1998-35052	19980305

AB A plasma etch method for forming a patterned Si contg. dielec. layer within a microelectronics fabrication. There is 1st provided a plasma reactor chamber. There is then fixed within the plasma reactor chamber a microelectronics fabrication. The microelectronics fabrication comprises: (1) a substrate employed within the microelectronics fabrication; (2) a metal layer formed over the substrate; (3) a Si contg. dielec. layer formed upon the metal layer; and (4) a patterned photoresist layer formed upon the Si contg. dielec. layer. There is then etched through use of a plasma etch method at a 1st plasma reactor chamber pressure while employing the patterned photoresist layer as a photoresist etch mask layer the Si contg. dielec. layer to form a patterned Si contg. dielec. layer while reaching and etching the metal layer to form an etched metal layer. The plasma etch method employs an etchant gas compn. comprising a F contg. etchant gas. Finally, there is pumped the plasma reactor chamber to a 2nd plasma reactor chamber pressure lower than the 1st plasma reactor chamber pressure for a time sufficient to attenuate formation of a metal-fluoropolymer residue layer upon the etched metal layer.
RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L51 ANSWER 14 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 1998:250681 CAPLUS
DN 128:303026
TI Shallow trench isolation (STI) method employing gap filling silicon oxide dielectric layer
IN Jang, Syun-ming; Chen, Ying-ho; Yu, Chen-hua
PA Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5741740	A	19980421	US 1997-873836	19970612

AB There is 1st provided a Si substrate having a trench formed in it. The Si substrate is thermally oxidized to form a thermal Si oxide trench liner layer within the trench. A conformal Si oxide intermediate layer is formed on the thermal Si **oxide** trench liner by **plasma** -enhanced CVD method employing a **silane** Si source material. Finally, a gap-filling Si oxide trench fill layer is formed on the conformal Si oxide intermediate layer by sub-atm.-pressure thermal CVD employing O3 and TEOS. To provide improved properties of the gap-filling Si oxide trench fill layer, the thermal Si oxide trench liner layer may be treated with a N-contg. plasma prior to forming the conformal Si oxide intermediate layer.

L51 ANSWER 15 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 1997:476123 CAPLUS
DN 127:89289
TI Method and apparatus for depositing antireflective coating
IN Cheung, David; Feng, Joe; Huang, Judy H.; Yau, Wai-Fan
PA Applied Materials, Inc., USA
SO Eur. Pat. Appl., 33 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 6

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 778496	A2	19970611	EP 1996-308857	19961205
	EP 778496	A3	19981014		
	EP 778496	B1	20020612		
	R: DE, GB				
	US 5968324	A	19991019	US 1996-672888	19960628
PRAI	US 1995-567338	A	19951205		
	US 1996-672888	A	19960628		

AB This invention provides a stable process for depositing an antireflective layer. Helium gas is used to lower the deposition rate of **plasma** -enhanced **silane oxide**, **silane** oxynitride, and **silane** nitride processes. Helium is also used to stabilize the process, so that different films can be deposited. The invention also provides conditions under which process parameters can be controlled to produce antireflective layers with varying optimum refractive index, absorptive index, and thickness for obtaining the desired optical behavior.

L51 ANSWER 16 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 1997:173073 CAPLUS
DN 126:232179
TI Making insulator structures for polysilicon resistors
IN Lee, Chung Kuang
PA Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5605859	A	19970225	US 1995-498355	19950705
	US 6215161	B1	20010410	US 1996-761883	19961209
PRAI	US 1995-498355	A3	19950705		

AB A polysilicon resistor structure for use within **integrated circuits** and a method by which the polysilicon resistor structure may be formed are described. A 1st insulating layer which is formed from a glassy material is formed directly on the surface of a **semiconductor** substrate. A polysilicon resistor is formed in contact with the 1st insulating layer. A 2nd insulating layer is formed directly on the 1st insulating layer and over the polysilicon resistor. The 2nd insulating layer is formed from Si **oxide** deposited by **plasma**-enhanced CVD using **silane** as the Si source material.

L51 ANSWER 17 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 1996:469918 CAPLUS
DN 125:156059
TI **Integrated circuit** manufacture
IN Jang, Syun-Ming; Liu, Lu-Min
PA Taiwan Semiconductor Manufacturing Co., Taiwan
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5536681	A	19960716	US 1995-494638	19950623

AB In manufg. an **integrated circuit** having **semiconductor device** structures in and on a **semiconductor** substrate, a conducting layer deposited overlying the top surfaces of the **semiconductor device** structures and patterned to form conducting lines with a gap between them, a 1st **silane**-based oxide layer is deposited over the conducting lines such that the gap remains between the conducting lines, and the 1st oxide layer is covered with a layer of photoresist which is patterned so that the portions of the 1st oxide layer overlying the conducting lines are not covered by the photoresist layer; the portions of the 1st oxide layer not covered by the photoresist layer are treated with N2 plasma; the photoresist layer is removed; and a 2nd oxide layer is deposited over the 1st oxide layer so that the gap is filled by the 2nd oxide layer; and fabrication of the **integrated circuit** is completed. The 1st oxide layer is formed by plasma-enhanced CVD from SiH4, and the 2nd oxide layer is formed by CVD from O3 and TEOS.

L51 ANSWER 18 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 1996:366153 CAPLUS
DN 125:73678
TI Method for selectively depositing silicon oxide spacer layers
IN Jang, Syun Ming; Yu, Chen Hua; Chen, Lung; Wu, Lin June
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5518959	A	19960521	US 1995-518706	19950824
	US 6329717	B1	20011211	US 1996-616140	19960314
PRAI	US 1995-518706	A3	19950824		

AB A method for selectively depositing a Si oxide insulator spacer layer between multilayer patterned metal stacks within an **integrated circuit** is described. Formed on a **semiconductor** substrate is a Si oxide insulator substrate layer which is formed by plasma-enhanced CVD. On the Si oxide insulator substrate layer are formed multilayer patterned metal stacks. The multilayer patterned metal stacks have a top barrier metal layer formed from **Ti nitride** and a lower-lying conductor metal layer formed from an **Al**-contg. alloy. Formed selectively on the portions of the Si oxide insulator substrate layer and on the edges of the **Al**-contg. alloy exposed through the multilayer patterned metal stacks is a Si oxide insulator spacer layer. The Si oxide insulator spacer layer is formed by O3-assisted CVD using TEOS as the Si source material. The Si oxide insulator spacer layer is formed for a deposition time not exceeding the incubation time for forming the Si oxide insulator spacer layer on the **Ti nitride** layer.

L51 ANSWER 19 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 1995:561756 CAPLUS
DN 122:304636
TI Manufacture of **semiconductor device**
IN Suzuki, Hiroshi
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 07066369	A2	19950310	JP 1993-210787	19930826

AB The title method involves the following steps; forming a dielec. film with high dielec. const. on a lower electrode, heating the film in an oxidizing atm., and forming an upper electrode on the film to form a memory capacitance part for very large scale **integrated circuits** (LSI) of dynamic random access memory (DRAM), etc. The device showed low leak current.

L51 ANSWER 20 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 1995:524134 CAPLUS
DN 122:303586
TI Manufacture of electrically insulating silica film by microwave plasma chemical **vapor deposition**
IN Shimizu, Akio
PA Fuji Electric Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 07050296	A2	19950221	JP 1993-196587	19930809

AB The title method involves the following steps; introducing O or N2O, SiH4 or Si2H6, and Ar into a microwave plasma reactor having a microwave generator, a cylindrical vacuum vessel, a solenoid coil, and a high-frequency power supply and growing a SiO2 film on a **semiconductor** substrate with supplying high-frequency elec. power. This method is useful for manuf. of SiO2 films as underlayer protecting films for multilayered wirings of **integrated circuits**.

L51 ANSWER 21 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 1991:73536 CAPLUS
DN 114:73536
TI Manufacture of **semiconductive integrated circuit** devices
IN Nakamura, Hiroyuki
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 02189921	A2	19900725	JP 1989-10509	19890118

AB In the title manuf., in which an **Al**-contg. material is used for the top layer of a single or multilayer circuit, the process involves **plasma-vapor-depositing** a Si oxide film over the entire surface of the top layer after circuit formation and subsequent sintering in H at 350-450.degree.. The deposition of the Si oxide prior the sintering protects the **Al** circuit from short circuits due to hillock formation on the exposed **Al** surface during the subsequent sintering.

L51 ANSWER 22 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 1985:587330 CAPLUS
DN 103:187330
TI Plasma-enhanced chemical **vapor deposition**
IN Hanssen, Johannes Hendrikus Leonardus
PA Neth.
SO Neth. Appl., 14 pp.
CODEN: NAXXAN
DT Patent
LA Dutch
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	NL 8303602	A	19850517	NL 1983-3602	19831019
	EP 143479	A1	19850605	EP 1984-201441	19841009
	R: AT, BE, CH, DE, FR, GB, IT, LI, LU, NL, SE				
PRAI	NL 1983-3602		19831019		

AB An app. for plasma-enhanced chem. **vapor deposition** involves a tube with an inlet and an outlet for gases and horizontal electrodes, acting as supports for the substrates to be coated, arranged in a vertical stack. Optionally, the set of electrode-supports is free from the tube wall. The electrodes may be partially coated with heat-resistant, elec. insulating material, e.g. quartz. The app. is used for deposition of Si3N4 by a plasma reaction of SiH4 and NH3, SiO2 by a reaction of SiH4 and N2O, and cryst. Si by pyrolysis of SiH4 or SiH2Cl2. The deposit may be doped with P, B, or As by addn. of the resp. hydrides to the reacting gases. The deposition processes are useful in the manuf. of photovoltaic cells, **semiconductor devices**, and resistors for **integrated circuits**.

L51 ANSWER 23 OF 23 CAPLUS COPYRIGHT 2002 ACS
AN 1974:431146 CAPLUS
DN 81:31146
TI Preparing a dielectric insulating layer in an epitaxial layer of a **semiconductor** compound
IN Sugano, Takuo; Mori, Yoshifumi
PA Hayashi, Kentaro
SO Ger. Offen., 15 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 2351395	A1	19740502	DE 1973-2351395	19731012
	DE 2351395	B2	19770505		
	DE 2351395	C3	19771222		
	JP 49060484	A2	19740612	JP 1972-102281	19721012
	GB 1424917	A	19760211	GB 1973-46860	19731008
	US 3935328	A	19760127	US 1973-405733	19731011
PRAI	JP 1972-102281		19721012		

AB Oxidizing gas plasma is used to form passivating layers on p-n and heterojunctions of **semiconductors** in **integrated circuits**. Thus, on a GaAs n-type substrate, an epitaxial 1-5 .mu.m layer is formed and then made p-type by Zn diffusion. The surface is next covered with **vapor-deposited Al** and the desired windows formed by using a photoresist. The unit is placed in a vacuum chamber equipped with a high frequency coil. At 0.3 torr O and 6-7 kV anode voltage, a plasma of 1000-1300.degree. is created to form a 10 .mu.m polycryst. oxide layer of 108-1010 .omega.-cm resistivity. For GaP and GaAs0.96P0.04 substrates 0.4-0.6 Torr O and 8 kV are used.

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File 349:PCT FULLTEXT 1983-2002/UB=20020801,UT=20020725
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STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

08/09/2002 09/805,027

Set	Items	Description
S1	14822	(SEMICONDUCT?????(N1)DEVICE? ?)/TI,AB,CM
S2	48484	SEMICONDUCT?????/TI,AB,CM
S3	40288	((INTEGRAT??????(3N)CIRCUIT? ?) OR IC)/TI,AB,CM
S4	398	(INTEGRAT??????(3N)DENSIT??????)/TI,AB,CM
S5	37328	(COPPER OR CU)/TI,AB,CM
S6	1015196	(ALUMINUM OR ALUMINIUM OR AL)/TI,AB,CM
S7	399	((TANTALUM OR TA)()(NITRIDE OR N))/TI,AB,CM
S8	12067	(SILANE OR SILICON()METHANE OR SIH)/TI,AB,CM
S9	355	(PLASMA(3N)OXIDE)/TI,AB,CM
S10	5325	(PVD OR (PLASMA()VAPOR()DEPOSIT??????) OR (VAPOR()DEPOSIT?-????))/TI,AB,CM
S11	569	(PECVD OR PLASMA()ENHANC????()CHEMICAL()VAPOR??????()DEPOSIT????)/TI,AB,CM
S12	106	(HDP OR HIGH()DENSITY()PLASMA()OXIDE)/TI,AB,CM
S13	4707	STUD??????(3N)(CONNECT?????? OR BRACE?????? OR LINK?????? OR CHAIN??????)
S14	11759	STUD??????/TI,AB,CM
S15	15183	S13:S14
S16	8686	(LINER? ? OR BARRIER? ?OR VIA()(LINER? ? OR BARRIER? ?))/TI,AB,CM
S17	2278	(INTERLAYER?????? OR INTER()LAYER??????)/TI,AB,CM
S18	53465	(INTERCONNECT?????? OR INTER()CONNECT??????)/TI,AB,CM
S19	3	((ELIMINAT?????? OR MINIMIZ?????? OR MINIMIS??????)(3N)((METAL??????(3N)MIGRAT??????)))/TI,AB,CM
S20	146	(METAL??????(3N)MIGRAT??????)/TI,AB,CM
S21	146	S19:S20
S22	48484	S1:S2
S23	40484	S3:S4
S24	1029622	S5:S8
S25	5775	S9:S11
S26	5847	S25,S12
S27	7044	S22 AND S23
S28	4886	S27 AND S24
S29	445	S28 AND S5
S30	359	S29 AND S6
S31	50	S30 AND S26
S32	8	S31 AND S15
S33	8	IDPAT (sorted in duplicate/non-duplicate order)
S34	8	IDPAT (primary/non-duplicate records only)
S35	42	S31 NOT S32
S36	2	S35 AND S16
S37	40	S35 NOT S36
S38	2	S37 AND S17
S39	2	S38 NOT S36
S40	38	S37 NOT S39
S41	19	S40 AND S18
S42	2	S41 AND S21

34/TI,PN,PD,PY,K/1 (Item 1 from file: 348)

Buried patterned conductor planes for **semiconductor**-on-insulator **integrated circuit**
Vergrabene strukturierte Leiterebenen fur einen integrierten Halbleiterschaltkreis auf einem Isolator
Plans de conducteur enterres a motifs pour un circuit integre base sur la technologie semi-conducteur sur isolant
PATENT (CC, No, Kind, Date): EP 948054 A2 991006 (Basic)

A **semiconductor**-on-insulator **integrated circuit** with buried patterned layers as **electrical** conductors for discrete device functions, **thermal** conductors, and/or decoupling capacitors.

...SPECIFICATION provide electrical connection between the substrate 12 or the implanted volumes 24A, 24B to the active devices 25A and 25B, typically about one (mu)m. **Stud** 34 **connects** source 30 of transistor 25A to Vdd)) through the substrate 12. **Stud** 35 **connects** source 30 of transistor 25B to ground in region 24B of Figures 5 and 6. Additional layers of dielectric 36 may then be deposited on...

2. The circuit of claim 1, wherein the first device is a first transistor and the first conductor is a first **stud** in **electrical** contact with the first transistor and wherein the second device is a second transistor and the second conductor is a second **stud** in **electrical** contact with the second transistor.

3. The circuit of claim 1, wherein the first voltage level is at Vdd)) and the second voltage level is...

..said circuit comprising an isolation volume between the first transistor and the second transistor; and said first and second conductors comprising first and second conductive **studs** electrically **connecting** respective transistors and volumes.

13. The circuit of claim 12, wherein the first conductive **stud** and the second conductive **stud** are made of **material** selected from the group consisting of tungsten, **copper**, **aluminum**, and doped silicon.

22. The method of Claim 17, wherein the step (e) of filling the isolation volumes with a fourth insulator further comprises **chemical vapor deposition** of silicon dioxide to provide **conformal** deposition.

24. The method of Claim 23, wherein the step (i) of introducing a conductive **material** into the **stud** opening further comprises:

(i1) coating the opening with a titanium compound to promote adhesion; and

(i2) conformally introducing tungsten into the **stud** openings by **chemical vapor deposition** of sputter

08/09/2002 09/805,027

34/TI,PN,PD,PY,K/2 (Item 2 from file: 348)

Diamond-like carbon for use in VLSI and ULSI interconnect systems
Diamantahnlicher Kohlenstoff zur Verwendung in VLSI und ULSI-Verbindungssystemen
Diamant de i-carbone pour des systemes d'interconnexion de VLSI et ULSI
PATENT (CC, No, Kind, Date): EP 696819 A1 960214 (Basic)

...ABSTRACT A1
The present invention relates to **semiconductor devices** comprising as one of their **structural** components diamond-like carbon (20) as an insulator for spacing apart one or more levels of a conductor (16,22) on an **integrated circuit** chip. The present invention also relates to a method for forming an integrated structure and to the integrated structure produced therefrom. The present invention further provides a method for selectively ion etching a diamond-like carbon layer (20) from a substrate (12) containing such a layer.

5. The insulator of the **semiconductor device** of any of the preceding claims 1 to 4 wherein the diamond-like carbon **material** is formed by a process selected from the group consisting of plasma assisted **chemical vapor deposition**, sputtering, ion beam deposition and laser ablation.

said first and second layers having **studs** of a second metal interconnecting selected ones of said first conductive regions and said first interconnect pattern.

8. The interconnect structure of claim 7 wherein...

...atoms of said fluorinated diamond-like carbon.

10. The interconnect structure of any of the preceding claims 7 to 9 wherein said diamond-like carbon **material** is hydrogenated amorphous carbon.

11. The interconnect structure of any of the preceding claims 7 to 10 wherein the first metal and the second metal are selected from the group consisting of **Al**, **Cu**, W and alloys thereof.

12. The interconnect structure of any of the preceding claims 7 to 11 further including a third metal layer between sidewalls...

34/TI,PN,PD,PY,K/3 (Item 3 from file: 348)

Copper germanium compounds capable of being produced at low temperature
Kupfer-Germanium Verbindungen, die bei Niedrigtemperatur hergestellt werden konnen
Composes cuivre-germanium pouvant etre produits a basse temperature
PATENT (CC, No, Kind, Date): EP 472804 A2 920304 (Basic)
EP 472804 A3 920624
EP 472804 B1 970730

Cu (14) is deposited as a film on the surface of a single crystalline **semiconductor** substrate (18) of Si or Ge, while the substrate is held at room temperature. It has been found that the materials will react by themselves over an extended period of time to form a **Cu**-silicide (20) or **Cu**-germanide (46) compound interface. The process may be used to produce interconnection metallization for **integrated circuits**, but, in the context of existing VLSI processes, heat is used to accelerate the formation using the minimum desirable parameters of a temperature of about 150(degree)C for about 20 minutes. Contrary to the belief in the art that **Cu** always diffuses in silicon, the resulting interface junction has been found to demonstrate superior (near **ideal**) current/voltage characteristics and can be used as a high temperature (600-800(degree)C) stability Ohmic/Schottky contact to Si or as a **Cu** diffusion barrier. **Additional** embodiments involve a **Cu** layer on a Ge layer on Si substrate, a **Cu** layer on a Si(sub(x))Ge(sub(1-x)) layer on Si substrate, and the use of an intermediate layer of a refractory metal such as W. Various other VLSI embodiments are also disclosed. (see image in **original** document)

...SPECIFICATION structure, of a form considered likely to be used for multilevel interconnect metallization, containing a void-open failure in the upper line just above the **connecting stud**
...**CLAIMS A3**
1. **A method of forming an interconnection metallization for integrated circuits** comprising the steps of:

depositing a layer of Ge(sub(x))Si(sub(1-x)) (49) on a **semiconductor** substrate (52);

depositing a layer of oxide (50) on said Ge(sub(x))Si(sub(1-x)) layer having a window therein;

depositing a layer (47) of a single crystalline **semiconductor** on the exposed surface of said Ge(sub(x))Si(sub(1-x)) layer in said window in said oxide layer;

depositing a layer of **Cu** (48) on said **semiconductor** layer; and

producing each of at least two tri-layer structures (60, 62) by

depositing layers of Ge and **Cu** using **chemical vapor deposition** (CVD) and adjusting the relative thicknesses to form **Cu**(sub 3)Ge/**Cu**/**Cu**(sub 3)Ge as the three layers;

34/TI,PN,PD,PY,K/4 (Item 4 from file: 348)

Semiconductor device having a diffusion barrier and process for its production.
Eine Diffusionsmembran enthaltende Halbleiterschaltung und deren Herstellungsverfahren.
Dispositif semi-conducteur incorporant une barriere de diffusion et son procede de fabrication.
PATENT (CC, No, Kind, Date): EP 248445 A2 871209 (Basic)
EP 248445 A3 881012

Semiconductor device having a diffusion barrier and process for its production.

...ABSTRACT A2
This invention provides a **semiconductor device** having an electrode conductor layer (6) on a **semiconductor** substrate (1) through the medium of a diffusion barrier layer (5) which is formed of an amorphous **material** having a higher crystallization temperature than the heat treatment temperature for the **semiconductor device**, and a process for manufacturing this device.

1. A **semiconductor device** comprising a **semiconductor** substrate (1) having **integrated circuits** therein, a diffusion barrier layer (5) formed on said substrate, and an electrode conductor layer (6) formed of **aluminum** or an **aluminum**-silicon alloy on said diffusion barrier layer (5), characterized in that the diffusion barrier layer (5) is formed of an amorphous **material** having a crystallization temperature which is higher than the temperature of the heat treatment applied to the **semiconductor device** after formation of the electrode conductor layer (6) (Fig. 1).

4. The **semiconductor device** according to one of claims 1 to 3, characterized in that the amorphous **material** of the diffusion barrier layer (5) is an alloy, or a compound, of at least two metals selected from beryllium, boron, silicon, titanium, manganese, iron, cobalt, nickel, **copper**, yttrium, zirconium, niobium, molybdenum, ruthenium, rhodium, palladium, hafnium, tantalum, tungsten, rhenium, iridium, thorium, samarium, gadolinium, and terbium.

principal steps:
(A) providing a **semiconductor** substrate (1),
(B) providing the respective doped regions (2, 3) of desired conductivity type and impurity/dopant concentration corresponding to the desired **integrated circuit** structures
(C) forming an insulating oxide film (4) on the surface of the **semiconductor** body including the desired contact holes,
that step (F) is carried out by dry etching.

23. The diffusion barrier layer (5) is deposited by **vapor deposition** or **chemical vapor deposition**.

25. The process according to one of claims 17 to 24, characterized in that in step (D) a combination of at least two of the following metals is used: beryllium, boron, silicon, titanium, manganese,

iron, cobalt, nickel, zirconium, niobium, molybdenum, **copper**, yttrium, ruthenium, rhodium, palladium, hafnium, tantalum, tungsten, rhenium, iridium, thorium, samarium, gadolinium, and terbium.

34/TI,PN,PD,PY,K/5 (Item 5 from file: 349)

SECURITY MODULE SYSTEM, APPARATUS AND PROCESS
SYSTEME MODULAIRE DE SECURITE, APPAREIL ET PROCEDE
Patent and Priority Information (Country, Number, Date):
Patent: WO 200159544 A2-A3 20010816 (WO 0159544)
Publication Year: 2001

. etching techniques or focused-]on beam methods.
U.S. Patent No. 5,389,738 describes electrode finger grids which are provided above and below an **integrated circuit** die to detect physical attempts to penetrate the **integrated circuit** die.
U.S. Patent No. 5,159,629 describes a screen material with fine conductive lines formed thereon in close proximity to each other. This...

...component assembly may be performed using chip-on-board (COB) technology for wirebondable die, or a combination of COB and SMT for passive components. The **integrated circuits** (ICs) may be attached to the substrate using conductive epoxy, and wirebonded with **aluminum** wire. The top surface finish required for the **aluminum** wirebonding is compatible with the use of Pb/Sn eutectic alloy. The use of gold wirebonding requires a thicker gold finish to the bond pads, which potentially creates reliability issues for the solder joints formed on the same surface. In addition, the use of **aluminum** wirebonds contribute to tamper protection because they do not produce X-ray contrast. The leads used to surface mount the security module in an SMT implementation of the present invention may be solder attached to the substrate. **Copper** leads may be used to match the coefficient of thermal expansion of the substrate. Lead attachment may be performed using high Pb content solder with...

...around the enclosed area. During the assembly process, selective wirebonding of the programmable pad array may be performed using, as an example, X-ray transparent **aluminum** wire. Thus, the programming of pseudo-random combinations of serial conductor paths around the enclosed area may be cost-effectively programmed into the automatic wirebonding...

...DLQ could be used in place of the security coating. DLC may be deposited over the electronic components using a low temperature plasma-assisted chemical **vapor deposition** (PACVD) process. DLC is a very hard, insulating, highly chemically inert compound with excellent adhesion to the silicon, metal, and dielectric surfaces, which may be...

34/TI,PN,PD,PY,K/6 (Item 6 from file: 349)

SEMICONDUCTOR PROCESSING SILICA SOOT ABRASIVE SLURRY METHOD FOR **INTEGRATED CIRCUIT** MICROELECTRONICS
MICRO-ELECTRONIQUE A CIRCUIT INTEGRES : TECHNIQUE DE TRAITEMENT DE SEMI-CONDUCTEURS AU MOYEN D'UNE SUSPENSION ABRASIVE A BASE DE SUIE DE SILICE
Patent and Priority Information (Country, Number, Date):
Patent: WO 200139260 A1 20010531 (WO 0139260)

English Abstract
The invention utilizes colloidal silica soot (62) in a **semiconductor** process for chemical-mechanical planarizing a **semiconductor integrated circuit** workpiece (24) with a slurry (60). The particulate abrasive agent colloidal solid sphere fused silica soot (62) provides a beneficial CMP slurry/process for **semiconductor device** manufacturing compared to standard **semiconductor** CMP slurries with conventional colloidal sol-gel or fumed silica.

SEMICONDUCTOR PROCESSING SILICA SOOT ABRASIVE SLURRY METHOD FOR **INTEGRATED CIRCUIT** MICROELECTRONICS
CROSS-REFERENCE TO RELATED APPLICATION
This application claims the benefit of priority of U.S. Provisional Application No. 60/167,12 1, filed November 23, 1999, entitled Silica Soot Abrasive For Microelectronic Materials, of Darcangelo et **al.**, which is hereby incorporated.
FIELD OF THE INVENTION
The present invention relates to planarization of a **semiconductor** substrate, and more particularly relates to chemical mechanical polishing (CMP) of **semiconductor integrated circuit** workpiece surfaces.
result in optimal **semiconductor** workpiece surface finish attainment. Particle size distribution can be I 0 adjusted.to control the final surface finish as well as the ability to clean residue abrasive particles from workpiece surfaces after processing. The present invention describes the application of colloidal silica soot produced as a byproduct of chemical **vapor deposition** processing of glasses in the **semiconductor integrated circuit** finishing industry, specifically for application to silicon wafers, oxide coating on such wafers, 1 5 conductive metals used in microelectronic devices (e.g., **aluminum**, **copper**, tantalum, tungsten, etc.). and ceramics used in microelectronics (e.g., silicon nitride and silicon carbide). The abrasive particles of a CMP slurry effect the slurry...

...Soot of the invention, a likewise adjustment can be made using a potassium-based buffer solution.
With regards to polishing of interconnecting metals in microelectronic **integrated circuit** devices (e.g., **aluminum**, **copper**, tantalum, tungsten, etc.) the soot materials offer advantages including (1) relatively large particle size (> 0.25 @tm) with spherical morphology and (2) added stabilization of TiO2-SiO2 over SiO2.

The inventive soot materials demonstrate four preferred points in specific application to the !momechanical polishing (planarization) of microelectronic materials such as **copper**, **aluminum**, tungsten, and silicon as well as related carbides and nitrides: First, the Ti doped soot shows significantly improved stability at low pH (< pH 5) as...

materials used in **semiconductor** circuit manufacturing including but not limited to a metal layer, a **semiconductor** such as silicon, a doped **semiconductor**, a polysilicon er, or a metal silicide layer. An interlayer dielectric (ILD) 30 is formed over conductive layer 42. Interlayer dielectric 30 is a thin film insulator which is generally an undoped silicon **dioxide** formed by **plasma** enhanced CVD of TEOS between

...one of a plurality of well-known techniques, including but not limited to, reactive sputtering from a titanium target in a nitrogen atmosphere and chemical **vapor deposition** (CVD). Titanium nitride layer 36 provides an adhesion layer and a difftision barrier for a subsequently deposited tungsten layer which is known to have poor adhesion to insulators like SiO2, and high reactivity with metals such as **aluminum** and niu

...preferably have an insolution stability with soot particles gellation resistant in slurry 60. In an embodiment soot particles 62 are coated with cerium, iron, zirconium, **aluminum**, or oxides formed thereof The invention includes a method of making a **semiconductor** processing

..by shear mixing. Slurry 60 and solvent preferably include chemical additives such as oxidizing agents, for example hydrogen 1 5 peroxide and nitric acid for **copper** dissolution, and inhibitors such as benzo-tri-azole (BTA). The method of making slurry 60 includes loading at least I wt. % of the soot, and...

...fused silica glass soot 62 is a Ge doped fused silica glass soot. In an embodiment the doped fused silica glass soot 62 is an **Al** doped fused silica glass soot. in embodiment the doped fused silica glass soot 62 is a B doped fused silica glass soot. In an embodiment...improved stability over pure undoped high purity SiO2. Providing soot particles 62 preferably includes collecting fused silica soot particles as a byproduct from a chemical **vapor deposition** glass making process. In a preferred embodiment collecting includes collecting high purity fused silica soot particles as an exhausted byproduct form a direct deposition high...

34/TI,PN,PD,PY,K/7 (Item 7 from file: 349)

METHOD AND APPARATUS FOR METAL OXIDE CHEMICAL **VAPOR DEPOSITION** ON A SUBSTRATE SURFACE
PROCEDE ET APPAREIL DE DEPOT CHIMIQUE EN PHASE VAPEUR D'OXYDE METALLIQUE SUR UNE SURFACE DE SUBSTRAT
Patent and Priority Information (Country, Number, Date):
Patent: WO 200054893 A1 20000921 (WO 0054893)
Publication Year: 2000

English Abstract
A method and apparatus for improved metal oxide chemical **vapor deposition** on a substrate surface where the application boundary layer is reduced and where the uniformity of the application boundary layer is greatly enhanced in a...

Claim
DETAILED DESCRIPTION OF THE PREFERRED EMBODIHEMTS
FIG. I illustrates the method and apparatus for Metal Oxide Chemical **Vapor Deposition** on a substrate surface. A downflow
reactor 10 apparatus is incorporated and utilized for Metal Oxide Chemical **Vapor Deposition** (MOCVD) upon the upper surface of a substrate 12 positioned central to the downflow reactor 10. The downflow reactor 10 is a cold wall vacuum...

Pla=2-enhanced CVD **PECVD** RF
Photolytic CVD LTVCVD Photons
Laser CVD LCVD Photons
CVD Systems
Deposition
Pressure Temperature
System Overall Reaction (Pasca@ (K)
Si EpitxxN **SiH** 4-IC11 + II 2 Si + xHC1, x = 0, 2, 3, or 4 101 kPa
1050-1450
Plasma silicon **dioxide** SiH4 + N-)o 200-350
LPCVO OF **ALUMINUM** AND **Al**-Si' ALLOYS
PYROLYSIS OF TRI-ISOBUTYL **ALUMINUM**, THEN ALLOYING:
AI(C4HS)3 200-30(rC **Al** + 3/2 H2 +3C4Ha
46(rC
Al + SiH4 **Al**-Si + 2
I I A method for improved chemical **vapor deposition** on a substrate surface where the application boundary layer is reduced and where the uniformity of the application boundary layer is greatly enhanced in a...

34/TI,PN,PD,PY,K/8 (Item 8 from file: 349)

HIGH PERFORMANCE CAPACITORS USING NANO-STRUCTURE MULTILAYER MATERIALS FABRICATION
CONDENSATEURS A HAUTE PERFORMANCE FABRIQUES A PARTIR DE MATERIAUX MULTICOUCHES A STRUCTURE NANOMETRIQUE
Patent and Priority Information (Country, Number, Date):
Patent: WO 9508831 A1 19950330
Publication Year: 1995
.contamination solids synthesized using atom by atom processes. They are characterized by a high concentration of material interfaces. The most notable of such materials as **semiconductor** superlattices fabricated using molecular beam epitaxy (MBE). However, multilayers may be synthesized using elements from all parts of the Periodic Table Using MBE, evaporation, sputtering and electrochemical deposition technologies. At this time, multilayer structures have been fabricated by physical **vapor deposition** from at least 75 of the 92 naturally occurring elements in elemental form, as alloys or as compounds. The structure of multilayer materials is determined... generally at 20 having a length (1) of 300mm, a width(w) of 200mm, and a thickness(t) of 1mm. Terminals or tabs, such as **copper** strips 21 and 22, layers 27 The conductive layers 26 are **copper** (**Cu**) and the dielectric layers ...such as titanium dioxide (TiO2), calcium titanate (CaTiO3), or zirconium dioxide (ZrO2) and fero-electric materials such as barium titanate (BaTiO3) may be used, and **aluminum** (**Al**) for example may be used as the conductive layers. The characteristics Of SiO2, used in this design embodiment are:

...interconnected or non-interconnected capacitors may be fabricated for use as fundamental integrated components for power supplies, power electronics, power distribution busses, electronics packaging, printed **circuit** boards **integrated circuit** packaging, and **circuit** interconnect in **integrated circuits**.

7 The capacitor of Claim 1, wherein said conductive material is selected from the group consisting of **copper**, **aluminum**, zirconium, and titanium, and wherein the dielectric material is selected from the group consisting of silicon dioxide, titanium dioxide, calcium titanate, zirconium ...section of about one-half the cross-section of another end of said layer.

34/TI,PN,PD,PY,K/8 (Item 8 from file: 349)

HIGH PERFORMANCE CAPACITORS USING NANO-STRUCTURE MULTILAYER MATERIALS FABRICATION
CONDENSATEURS A HAUTE PERFORMANCE FABRIQUES A PARTIR DE MATERIAUX MULTICOUCHES A STRUCTURE NANOMETRIQUE
Patent and Priority Information (Country, Number, Date):
Patent: WO 9508831 A1 19950330
Publication Year: 1995
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naturally occurring elements in elemental form, as alloys or as compounds. The structure of multilayer materials is determined... generally at
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layers
27 The conductive layers 26 are **copper** (**Cu**) and the dielectric layers ...such as titanium dioxide (TiO2), calcium titanate (CaTiO3), or
zirconium dioxide (ZrO2) and fero-electric materials such as barium titanate (BaTiO3) may be used, and **aluminum** (**Al**) for example may be
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...interconnected or non-interconnected
capacitors may be fabricated for use as fundamental integrated components for power supplies, power electronics, power distribution busses, electronics packaging, printed **circuit** boards
integrated circuit
packaging, and **circuit** interconnect in **integrated circuits**.

7 The capacitor of Claim 1, wherein said conductive material is selected from the group consisting of **copper**, **aluminum**, zirconium, and
titanium, and wherein the dielectric material is selected from the group consisting of silicon dioxide, titanium dioxide, calcium titanate, zirconium ...section of about one-half the cross-section of another end of said layer.

36/TI,PN,PD,PY,K/1 (Item 1 from file: 348)

08/09/2002 09/805,027

Semiconductor cavity filling process
Verfahren zum Fullen eines Halbleiterhohlraumes
Procede pour obturer une cavite dans un semi-conducteur
PATENT (CC, No, Kind, Date): EP 731503 A2 960911 (Basic)
EP 731503 A3 971029

Semiconductor cavity filling process

...ABSTRACT A2
An improved process is provided which allows for enhanced filling of contacts, vias (600 and trenches (80) that are formed in dielectrics (62) of **integrated circuits**, particularly sub-0.5 (mu)m technologies. In a preferred aspect of the invention, filling proceeds at a temperature of about 250(see image in **original** document)(see image reference in **original** document)-450(see image reference in **original** document) in a vacuum of about 10(sup(-6) - 10(sup(-8) TORR and a processing pressure of about 300 - 1,000 atmospheres. The process of the present invention is applicable for different metals and metal alloys, adjustments to the processing parameters being undertaken in accordance with the various **chemical** and **physical** properties of the **material** to be filled in the respective contacts, vias (60) or trenches (80). (see image in **original** document) ...

...4. The process according to claim1, wherein said metal is slected from a group consisting essentially of one or more of the following compositions: (1) **Al**-Ti (0.1%) - **Cu** (0.5%); (2) **Al** - **Cu** (0.5%); (3) **Al** - **Cu** (1%); (4) **Al** - Si (1%) - **Cu** (0.5%); (5) **Aluminum**; (6) **Copper**; (7) alloys of **Cu** with one or more of the follwing metals: (I) Mg, (ii) Au, and (iii) Ag; (8) **Al** - Sc - **Cu**; (9) Ti; (10) TiN; and (11) combinations of Ti with one or more of the following: TiN, TiW and W.

...levels consisting essentially of different ones of said recited polymeric insulators.

8. The process according to claim 5, wherein said aperture provided with a metal **liner** that is applied aby one of a **chemical** vapor or **physical vapor deposition** process.

9. The process according to claim 8, wherein said aperture is inthe form of a via so as to extend from an upper level...

13. The process according to claim 1, furhter comprising the step of applying a dielectric **liner** to said aperture prior to the application of metal to said aperture.

14. The process according to claim 1, wherein said pressure is applied while said **semiconductor** body surface is exposed to an atmosphere containing an inert element.

15. The process according to claim 1, wherein said aperture is formed in a dielectric **material** and is provided with a metal **liner** that is applied by one of a **chenical** vapor or

physical vapor deposition process.
preceding claim.

22. An **integrated circuit** including a silicon body as claimed in claim 21.

08/09/2002 09/805,027

36/TI,PN,PD,PY,K/2 (Item 1 from file: 349)
DIALOG(R)File 349:(c) 2002 WIPO/Univentio. All rts. reserv.

INTEGRATED CIRCUIT INTERCONNECT LINES HAVING SIDEWALL LAYERS
LIGNES DE CONNEXIONS DE CIRCUITS INTEGRES AVEC COUCHES DE PAROIS LATERALES
Patent and Priority Information (Country, Number, Date):
Patent: WO 200005773 A1 20000203 (WO 0005773)
Publication Year: 2000
English Abstract
The present invention provides **Cu** lines which are enclosed within **Cu** diffusion barrier layers, for **IC** structures such as **semiconductor devices**. The **Cu** lines (310) have conventional top (316) and bottom (318) **Cu** diffusion barrier layers and novel sidewall layers (324 and 326) comprising **Cu** diffusion barrier materials. The present invention also provides for conductive interconnect lines for **semiconductor devices** which compensate partly or completely for a misalignment between the line etch pattern and the underlying contact element, such as a via plug. The misalignment...

a) forming a **Cu** containing sandwich line on the dielectric layer, wherein the sandwich line comprises: (1) a first **Cu** diffusion barrier layer comprising a top **Cu** barrier layer, (2) a second **Cu** diffusion barrier layer, comprising a bottom **Cu** barrier layer, formed on the dielectric layer, (3) a **Cu** containing layer interposed between the top **Cu** barrier layer and the bottom **Cu** barrier layer, (4) a first side surface extending along a first side of the sandwich line and (5) a second side surface
11 The method of claim I wherein the **Cu** difflusion barrier sidewalls comprise one or more **Cu** diffusion barrier materials selected from the group consisting of CVD TiN, CVD WN, CVD Ta, CVD TaN, CVD TaSiN, **PVD** TiN, **PVD** WN, **PVD** Ta, **PVD** TaN, **PVD** TaSiN, CVD silicon nitride, **PECVD** Si,,NYH, CVD SiOYNx, **PECVD** SiOYN,,, **PECVD** SiC and CVD amorphous carbon.
12 The method of claim I wherein the top and bottom **Cu** difflusion barrier layers comprise one or more **Cu** diffusion barrier materials selected from the group consisting of CVD TiN, CVD WN, CVD Ta, CVD TaN, CVD TaSiN, **PVD** TiN, **PVD** WN, **PVD** Ta, **PVD** TaN and **PVD** TaSiN.
a) depositing a **liner** on the dielectric layer; b) depositing a conductive layer, contacting the contact element, on the **liner**, c) depositing a line mask, overlaying the contact element, on the conductive layer;
30 The method of claim 29 wherein the misalignment tolerant sidewalls comprise one or more materials selected from the group consisting of CVD TiN, CVD WN, CVD Ta, CVD TaSiN, CVD TaN, **PVD** TiN, **PVD** WN, **PVD** Ta, **PVD** TaSiN, **PVD** TaN, CVD silicon nitride, **PECVD** Si,,NYH,, CVD SiOYN, **PECVD** SiOYN, . **PECVD** SiC and CVD amorphous carbon.

39/TI,PN,PD,PY,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

High performance system-on-chip using post passivation process
Hochleistungssystem auf einem Chip unter Verwendung eines Verfahrensschrittes nach einem Passivierungsschritt
Systeme a haute performance sur un chip utilisant un procede apres une etape de passivation
PATENT (CC, No, Kind, Date): EP 1209725 A2 020529 (Basic)

1. A method for forming an inductor for high performance **integrated circuits** overlaying the surface of a **semiconductor** substrate, comprising:
providing a **semiconductor** substrate, in or on the surface of which **semiconductor devices** have been created, having points of **electrical** contact provided to said **semiconductor devices** in or on the active surface of said substrate;
creating an overlaying interconnecting metalization structure comprising one or more layers of interconnects over the active...

depositing a polymer insulating, separating layer over said passivation layer that is substantially thicker than said passivation layer and that is also substantially thicker than an **inter-layer** dielectric used for creating said interconnecting metallization structure;

3. The method of claim 1 wherein said points of **electrical** contact having been provided in or on the surface of said overlaying interconnecting metalization structure comprise a **material** that is selected from a group comprising sputtered **aluminum**, CVD tungsten, CVD **copper**, electroplated gold, electroplated silver, electroplated **copper**, electroless gold and electroless nickel.

4. The method of claim 1 whereby said inductor is embedded in a dielectric and furthermore covered by a layer...

16. The method of claim 15 wherein said passivation layer comprises a layer within the range of approximately 0.15 to 2.0 (mu)m of **Plasma** Enhanced CVD (**PECVD**) **oxide** over which a layer within the range of approximately 0.5 to 2.0 (mu)m **PECVD** nitride is deposited.

17. The method of claim 15 wherein said polymer i
nitride is deposited.

50. A resistor for high performance **integrated circuits** on the surface of a **semiconductor** substrate, comprising:
a **semiconductor** substrate, in or on the surface of which **semiconductor devices** have been created, having points of **electrical** contact provided to said **semiconductor devices** in or on the active surface of said substrate;
an overlaying interconnecting metalization structure comprising one or more layers of interconnects over the active surface...

64. The discrete **electrical** component of claim 63 wherein said passivation layer comprises a layer within the range of approximately 0.15 to 2.0 (mu)m of **Plasma** Enhanced CVD (**PECVD**) **oxide** over which a layer within the range of approximately 0.5 to 2.0 (mu)m **PECVD** nitride is deposited.

65. The discrete **electrical** component of cl

08/09/2002 09/805,027

39/TI,PN,PD,PY,K/2 (Item 1 from file: 349)
DIALOG(R)File 349:(c) 2002 WIPO/Univentio. All rts. reserv.

DEEP SUBMICRON METALLIZATION USING DEEP UV PHOTORESIST
METALLISATION PROFONDE SUBMICROMIQUE A L'AIDE DE PHOTORESIST POUR ULTRAVIOLETS LOINTAINS
Patent and Priority Information (Country, Number, Date):
Patent: WO 9954930 A1 19991028
Publication Year: 1999

English Abstract
Reflection of incident optical radiation from a highly reflective metal layer (12), such as **aluminum**, **copper** or titanium, into a photoresist layer (16) is reduced by interposing a layer of silicon oxynitride (14) between the metal and photoresist layers. The silicon...

3 The method defined in claim 1, wherein the first metallization layer (12) comprises **aluminum**.

4 The method defined in claim 1, wherein the first metallization layer (12) comprises **copper**.
5 . The method defined in claim 1, wherein the thickness and chemical composition of the silicon oxynitride layer (14) are selected to allow for strong...

...The method defined in claim 1, further comprising the step of planarizing the dielectric layer (20).
9 The method defined in claim 1, wherein the **interlayer** opening (40)
comprises a via.

13 The method defined in claim 1, wherein the first metallization layer (12) is deposited using **plasma enhanced chemical vapor deposition**.
1 5 14. The method defined in claim 1, wherein the method is repeated to create successive layers of interconnect.

15 A deep submicron **semiconductor integrated circuit** interconnect

42/TI,PN,PD,PY,K/1 (Item 1 from file: 349)
DIALOG(R)File 349:(c) 2002 WIPO/Univentio. All rts. reserv.

METAL ION DIFFUSION BARRIER LAYERS
COUCHE D'ARRET DE DIFFUSION D'IONS METALLIQUES
Patent and Priority Information (Country, Number, Date):
Patent: WO 200254484 A2 20020711 (WO 0254484)
Publication Year: 2002

English Abstract

An **integrated circuit** comprising a subassembly of solid state devices formed into a substrate made of a **semiconducting** material. The devices within the subassembly are connected by metal wiring formed from conductive metals. A diffusion barrier layer of an alloy film having the...

2 The **integrated circuit** as claimed in claim I wherein the diffusion barrier layer is produced by chemical **vapor deposition**.

13 A method of preventing **migration** of **metal** ions between adjacent device **interconnections** in an electrical circuit having metal wiring by applying over at least the metal wiring a diffusion barrier layer of an alloy film having the...

22 The method as claimed in claim 21 wherein the metal wiring is **aluminum**.

23 The method as claimed in claim 22 wherein the metal wiring is **copper**.
14

42/TI,PN,PD,PY,K/2 (Item 2 from file: 349)

METHODS AND APPARATUS FOR ELECTROPOLISHING METAL **INTERCONNECTIONS** ON **SEMICONDUCTOR DEVICES**
PROCEDES ET APPAREIL D'ELECTROPOLISSAGE D'INTERCONNEXIONS METALLIQUES DE DISPOSITIFS SEMI-CONDUCTEURS
Patent and Priority Information (Country, Number, Date):
Patent: WO 200003426 A1 20000120 (WO 0003426)
Publication Year: 2000

substrate layer 124 preferably includes silicon. It should be recognized, however, that substrate layer 124 can include various **semiconductor** materials, such as gallium arsenide and the like, depending on the particular application. 9. **Semiconductor** wafer 3 1, according to another aspect of the present invention, suitably includes a dielectric layer 123 formed on top of substrate layer 124. In...

...layer 123 preferably includes silicon dioxide (SiO2). Dielectric layer 123 can be formed on substrate layer 124 using any convenient deposition method, such as chemical **vapor deposition**, evaporation, sputtering, and the like.

...Fig. 1A, barrier layer 122 also suitably lines the walls of trenches 125. As will be described below, when a metal layer 121, which includes **copper**, is formed on top of dielectric layer 123, barrier layer 122 suitably prevents the **copper** in metal layer 121 from diffusing into dielectric layer 123. Accordingly, in the present exemplary embodiment, barrier layer 122 preferably includes material resistant to the diffusion of **copper**, such as titanium, tantalum, tungsten, titanium-nitride, **tantalum-nitride**, tungsten-nitride, and the like. Barrier layer 122 can be deposited using any convenient deposition method, such as physical **vapor deposition** (**PVD**), chemical **vapor deposition** (CVD), and the like. It should be recognized, however, that barrier layer 122 can be omitted in some applications. For example, when dielectric layer 123 is formed from a material, which is resistant to diffusion of **copper**, or when the 10. diffusion of **copper** into dielectric layer 123 will not adversely affect the performance of the **semiconductor device**. As alluded to above, depending on the particular application, metal layer 121, according to yet another aspect of the present invention, can be suitably formed...
of barrier layer 122 is typically about 5 0 to about I 00 times greater than the resistance of metal layer 12 1...1 0 medium, such as on magnetic tape, magnetic disk, compact disk, and the like, or in an appropriate electronic device, such as on an **integrated circuit**, memory chip, and the like. The control system can then execute appropriate commands to continue or to stop the electropolishing of a particular portion of...can contribute to the I 0 formation of recesses 127 within trenches 125. The existence of recesses 127 can adversely affect the perfortnance of the **semiconductor devi**

31 The method of claim I 1, wherein said barrier layer includes titanium, titanium-nitride. tantalum, tantalum-nitride, tungsten, or

tungsten-nitride.

32 The method of claim 1, further comprising the step of rotating the wafer while the electrolyte and polishing current are...

...The method of claim 35, wherein said orthophosphoric acid has a concentration of about 60 percent to about 85 percent and contains about I percent **aluminum** metal (against weight of the acid).

08/09/2002 09/805,027

09aug02 13:29:04 User267149 Session D270.1

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SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2002/Aug W1
         (c) 2002 Institution of Electrical Engineers
*File   2: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   6:NTIS  1964-2002/Aug W3
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removal, customized scheduling. See HELP ALERT.
  File   8:Ei Compendex(R)  1970-2002/Aug W1
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*File   8: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File  34:SciSearch(R) Cited Ref Sci  1990-2002/Aug W2
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removal, customized scheduling. See HELP ALERT.
  File 434:SciSearch(R) Cited Ref Sci  1974-1989/Dec
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  File  35:Dissertation Abs Online  1861-2002/Jul
         (c) 2002 ProQuest Info&Learning
  File  65:Inside Conferences  1993-2002/Aug W1
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  File  77:Conference Papers Index  1973-2002/Jul
         (c) 2002 Cambridge Sci Abs
  File  94:JICST-EPlus  1985-2002/Jun W2
         (c)2002 Japan Science and Tech Corp(JST)
*File  94: There is no data missing. UDs have been adjusted to reflect
 the current months data. See Help News94 for details.
  File  99:Wilson Appl. Sci & Tech Abs  1983-2002/Jun
         (c) 2002 The HW Wilson Co.
  File 108:Aerospace Database  1962-2002/Jul
         (c) 2002 AIAA
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  File 238:Abs. in New Tech & Eng.  1981-2002/Jul
         (c) 2002 Reed-Elsevier (UK) Ltd.
  File 305:Analytical Abstracts  1980-2002/Jul W4
         (c) 2002 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs  1970-2002/Jun
         (c) 2002 DECHEMA
  File 350:Derwent WPIX  1963-2002/UD,UM &UP=200249
         (c) 2002  Thomson Derwent
*File 350: Alerts can now have images sent via all delivery methods.
See HELP ALERT and HELP PRINT for more info.
  File 344:Chinese Patents Abs  JuL 1985-2002/JuL
         (c) 2002 European Patent Office
  File 347:JAPIO  Oct 1976-2002/Apr(Updated 020805)
         (c) 2002 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
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STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

08/09/2002 09/805,027

Alerts have been run. See HELP NEWS 347 for details.
File 371:French Patents 1961-2002/BOPI 200209
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*File 371: This file is not currently updating. The last update is 200209.

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

```
Set     Items   Description
S1     594181   (SEMICONDUCT?????(N1)DEVICE? ?)
S2    2426794   SEMICONDUCT?????
S3       7256   CC=B2560                Semiconductor devices
S4       4923   MC=S01-G02B
S5      98950   IC=G01R-031
S6    2504253   S1:S5
S7     909117   (INTEGRAT??????(3N)CIRCUIT? ?) OR IC
S8      35193   INTEGRAT??????(3N)DENSIT??????
S9     918654   S7:S8
S10   1421256   COPPER OR CU
S11   2787141   ALUMINUM OR ALUMINIUM OR AL
S12      5362   (TANTALUM OR TA)(1N)(NITRIDE OR N)
S13     37603   (TITANIUM OR TI)(1N)(NITRIDE OR N)
S14    132783   SILANE OR SILICON()METHANE OR SIH
S15      8599   PLASMA(3N)OXIDE
S16    242037   PVD OR (PLASMA()VAPOR()DEPOSIT??????) OR (VAPOR()DEPOSIT??-
           ????)
S17     59997   STUD??????(3N)(CONNECT?????? OR BRACE?????? OR LINK?????? -
          OR CHAIN??????)
S18     75440   LINER? ? OR VIA()LINER? ?
S19     82344   INTERLAYER?????? OR INTER()LAYER??????
S20    378714   INTERCONNECT?????? OR INTER()CONNECT??????
S21        29   (ELIMINAT?????? OR MINIMIZ?????? OR MINIMIS??????)(3N)((ME-
          TAL??????(3N)MIGRAT??????))
S22      4266   METAL??????(3N)MIGRAT??????
S23      4266   S21:S22
S24     23948   (SIGNAL??????(3N)PROPAGAT??????)
S25   4093770   S10:S14
S26    255407   S6 AND S9
S27     19829   S26 AND S25
S28      5335   S27 AND S10
S29      1652   S28 AND S11
S30         9   S29 AND S15
S31         9   RD (unique items)
S32         9   IDPAT (sorted in duplicate/non-duplicate order)
S33         8   IDPAT (primary/non-duplicate records only)
S34      1643   S29 NOT S30
S35       119   S34 AND S16
S36         0   S35 AND S17
S37         2   S35 AND S18
S38       117   S35 NOT S37
S39        10   S38 AND S19
S40        10   RD (unique items)
S41         3   IDPAT (sorted in duplicate/non-duplicate order)
S42         3   IDPAT (primary/non-duplicate records only)
S43         7   S40 NOT S42
S44       107   S38 NOT S39
S45        44   S44 AND S20
S46         0   S45 AND S23
S47         1   S45 AND S24
S48        43   S45 NOT S47
S49         8   S48 AND S12
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S50	8	RD (unique items)
S51	7	IDPAT (sorted in duplicate/non-duplicate order)
S52	7	IDPAT (primary/non-duplicate records only)
S53	35	S48 NOT S50
S54	6	S53 AND S13
S55	6	RD (unique items)
S56	5	IDPAT (sorted in duplicate/non-duplicate order)
S57	5	IDPAT (primary/non-duplicate records only)
S58	29	S53 NOT S54
S59	3	S58 AND S14
S60	26	S58 NOT S59
S61	0	S60 AND S14
S62	0	S60 AND S15
S63	26	S60 AND S16
S64	0	S60 AND S17
S65	0	S60 AND S18
S66	0	S60 AND S19
S67	24	RD S60 (unique items)
S68	6	IDPAT (sorted in duplicate/non-duplicate order)
S69	6	IDPAT (primary/non-duplicate records only)

33/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013506739
WPI Acc No: 2000-678683/200066
XRAM Acc No: C00-206325
XRPX Acc No: N00-502381
Fabrication of an **integrated circuit** involves doing special patterning process on the second etch stop layer by partially removing the etch stop barrier over the via and leaving the second etch stop barrier for trench
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: SHUE S; TSAI M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6133144	A	20001017	US 99368864	A	19990806	200066	B

Priority Applications (No Type Date): US 99368864 A 19990806
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6133144	A		11	H01L-021/4763	

Abstract (Basic): US 6133144 A
Abstract (Basic):
NOVELTY - An **integrated circuit** is fabricated on a substrate by performing a special patterning process on the second etch stop layer on top of the first intermetal dielectric layer (IMD) deposited over the first etch layer on top of the first level wiring layer and insulating layer. The stop layer material is removed over the via and patterned so that a stop layer material is left in trench areas.

DETAILED DESCRIPTION - Fabrication of the **integrated circuit** on the substrate (10) involves performing a special patterning process on the second etch stop layer on top of the first intermetal dielectric layer (IMD) (17) deposited over the first etch layer (16) on top of the first level wiring layer and insulating layer (14). The second etch stop layer material is removed over the via and patterned so that a stop layer material is left in trench or channel areas. A second IMD (30) is deposited over the patterned etch barrier which is patterned and etched to form special interconnect/via structures (44) and interconnect structures (46). The remnant etch stops are removed by a selective etch process. A channel and via barrier liner material is deposited in addition to the conducting material. The excess is polished back using chemical mechanical polishing. The process steps are repeated to construct multilevel conducting layers. The substrate where the **integrated circuit** is fabricated has a layer dielectric, interlevel dielectric (11), an interconnect line layer, or device contact region to P-N junctions.

USE - For fabricating **integrated circuits**, unique interconnect conducting lines, and via contact structures.

ADVANTAGE - The process produces well-defined, special low parasitic capacitance structures. It produces a reliable product with superior lines and via contact structures. It also reduces processing time and cost of ownership.

DESCRIPTION OF DRAWING(S) - The figure shows the formation of interconnect/via and interconnect wiring structures.

Substrate (10)
Interlevel dielectric (11)
Insulating layer (14)
First etch layer (16)
First intermetal dielectric layer (IMD) (17)
Second IMD (30)
Interconnect/via structures (44)
Interconnect structures (46)
pp; 11 DwgNo 4/4

33/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013506688
WPI Acc No: 2000-678632/200066
XRAM Acc No: C00-206294
XRPX Acc No: N00-502342
Formation of **aluminum** bump on an **integrated circuit** chip involves forming a composite dielectric layer of a spin-on-glass layer and **plasma** enhanced **oxide** layer over a passivation layer of a substrate
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: CHIEN W; LO C; YU D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6130149	A	20001010	US 99374298	A	19990816	200066	B

Priority Applications (No Type Date): US 99374298 A 19990816
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6130149	A		9	C23C-003/02	

Abstract (Basic): US 6130149 A
Abstract (Basic):
NOVELTY - An **aluminum** bump is formed by forming a composite dielectric layer (270) over a passivation layer (220) of a silicon substrate (200). The composite dielectric layer has a spin-on-glass layer and a **plasma** enhanced **oxide** layer. The silicon substrate has the composite passivation layer that covers a metal top layer.
DETAILED DESCRIPTION - Formation of an **aluminum** bump comprises forming a composite dielectric layer over a passivation layer of a silicon substrate, forming an opening through the composite dielectric and the passivation layers to expose a top metal layer (210) portion, forming a bump metal over the substrate to cover the opening portion of the top metal layer, forming a hard-mask over the bump metal, patterning the hard-mask to form a metal bump in the underlying the bump metal and removing the composite dielectric layer over the passivation layer. The composite dielectric layer has a spin-on-glass (SOG) layer and a **plasma** enhanced **oxide** (PEOX) layer. The silicon substrate has the composite passivation layer that covers the metal top layer.
USE - For forming **aluminum** bump on an **integrated circuit** chip.
ADVANTAGE - The inventive method prevents the entry of metal into the inclusions (223) by providing a sacrificial SOG layer that is formed before depositing the **aluminum** layer over the passivation layer. It provides **aluminum** bump on the **integrated circuit** chip without leaving any **aluminum** residue on the passivation layer of the chip.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view

of a portion of a **semiconductor** substrate showing the formation of **aluminum** bump.
Substrate (200)
Metal layer (210)
Passivation layer (220)
Inclusions (223)
Composite dielectric layer (270)
pp; 9 DwgNo 3f/3

33/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013474601
WPI Acc No: 2000-646544/200062
Related WPI Acc No: 2002-081834
XRAM Acc No: C00-195479
XRPX Acc No: N00-479131

Fabrication of fuse structures for **semiconductor integrated circuits**, involves depositing two polysilicon layers, and patterning the layers to form portions of the devices and levels of electrical interconnections

Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: HUANG K C; LEE Y H; SHIH C Y; WU C; YING T
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6121073	A	20000919	US 9824479	A	19980217	200062	B

Priority Applications (No Type Date): US 9824479 A 19980217
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6121073	A		10	H01L-021/82	

Abstract (Basic): US 6121073 A
Abstract (Basic):

NOVELTY - Fuse structures for **semiconductor integrated circuits** are fabricated by depositing two polysilicon layers; and patterning the polysilicon layers to form portions of the devices and levels of electrical interconnections over the fuses to provide an etch-stop layer.

DETAILED DESCRIPTION - Fabrication of fuse structures for **semiconductor integrated circuits**, comprises:

(a) providing a **semiconductor** substrate (10) having devices in device areas surrounded by a field oxide isolation (12);

(b) depositing a first polysilicon layer (14);

(c) patterning the first polysilicon layer to form portions of the devices and a first level of electrical interconnections, and further forming portions for fuses in the first level of electrical interconnections over the field oxide isolation;

(d) depositing an interpolysilicon oxide layer (16) over the patterned first polysilicon layer;

(e) depositing a second polysilicon layer (18);

(f) patterning the second polysilicon layer to form second level of electrical interconnections, and further having portions of the second polysilicon layer over the fuses to provide an etch-stop layer;

(g) depositing over the substrate an interlevel dielectric layer (20) having via holes with interconnecting metal plugs;

(h) depositing and patterning a metal layer over the interdielectric layer to form the next level of electrical interconnections;

(i) carrying out steps (g) through (h) n times to complete the metal interconnections for the **semiconductor integrated**

circuits, where the number of metal levels is n, and where n is at least 1;

(j) depositing a barrier layer on the substrate;

(k) coating a spin-on glass layer on the barrier layer;

(l) depositing a passivation layer on the spin-on glass layer;

(m) etching openings through the passivation layer, and through the interlevel dielectric layers to the etch-stop layer over fuses; and

(n) removing completely the etch-stop layer to complete the fuse structures having the interpolysilicon layer that is uniformly thick across the substrate over the fuses.

USE - For fabricating fuse structures used in **semiconductor integrated circuits**, e.g. random access memory (RAM) devices.

ADVANTAGE - The method allows fuse structures to be built without over etching that can cause fuse damage. The uniform thick insulating layer allows repeatable and reliable laser abrading (evaporation) to open the desired fuses. The method provides a more reliable repaired yield process for increasing the final product yield, and provides a cost-effective manufacturing process.

DESCRIPTION OF DRAWING(S) - The drawing shows a schematic cross-section of the processed fused structure.

substrate (10)

field oxide isolation (12)

first polysilicon layer (14)

inter polysilicon oxide layer (16)

second polysilicon layer (18)

interlevel dielectric layer (20)

pp; 10 DwgNo 4/5

33/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013279025
WPI Acc No: 2000-450960/200039
XRAM Acc No: C00-137365
XRPX Acc No: N00-335674
Diffusion barrier formation for encapsulating **copper** in **semiconductor device**, includes heating metal precursor gas to react with dielectric layer to form thin diffusion barrier
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: HONG Q; HSU W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6077774	A	20000620	US 97820744	A	19970319	200039	B

Priority Applications (No Type Date): US 97820744 A 19970319
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6077774	A		5	H01L-021/283	

Abstract (Basic): US 6077774 A
Abstract (Basic):
NOVELTY - A diffusion barrier is formed around a metal conductor in a **semiconductor device** by heating a metal precursor gas that is introduced into the surface of the dielectric layer to form relatively thin diffusion barriers.
DETAILED DESCRIPTION - Forming diffusion barrier around a metal conductor in a **semiconductor device** comprises flowing a metal precursor gas onto a surface of a dielectric layer. The metal precursor gas and the dielectric are then heated to a predetermined temperature to react metal atoms for the metal precursor gas with the dielectric to form a diffusion barrier having a material of metallic oxides and/or metallic carbides on the surface of the dielectric layer.

USE - For forming ultra thin and conformal diffusion barriers encapsulating **copper** in a **semiconductor integrated circuit** device.
ADVANTAGE - Provides an ultra thin, yet reliable and conformal diffusion barriers in a trench or via so that precise regulation of the reaction time to control the thickness is unnecessary, while the metal conductor is capable of carrying more current. The self-alignment of the barriers to selected surfaces during formation does not require extra-steps of processing to remove the diffusion barrier material from the other surfaces.
pp; 5 DwgNo 0/1

33/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013097618
WPI Acc No: 2000-269490/200023
XRAM Acc No: C00-082230
XRPX Acc No: N00-201674
Keyhole free **integrated circuit** device formation, comprises forming second high density **plasma oxide** layer over first to fill gap between conducting lines
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: LEE Y; WU C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6033981	A	20000307	US 99358988	A	19990722	200023	B

Priority Applications (No Type Date): US 99358988 A 19990722
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6033981	A		9	H01L-021/4763	

Abstract (Basic): US 6033981 A
Abstract (Basic):
NOVELTY - The formation **integrated circuit** keyhole is eliminated by:
(a) depositing first high density **plasma** (HDP) **oxide** layer over conducting lines and substrate;
(b) isotropic etching first HDP oxide layer and depositing insulating layer on it;
(c) removing insulating layer;
(d) etching exposed areas of the first HDP oxide layer;
(e) removing the insulating layer;
(f) forming insulating spacers; and
(g) depositing second HDP oxide layer
DETAILED DESCRIPTION - The formation of voids (keyhole), in a gap between closely spaced conducting lines, in an **integrated circuit** is eliminated by:
(i) providing a substrate (10);
(ii) providing the closely spaced conducting lines (30) having the gap;
(iii) depositing a first HDP oxide layer (14) over tops and sidewalls of the conducting lines and substrate;
(iv) isotropically etching the first HDP oxide layer;
(v) depositing an insulating layer over the first HDP oxide layer and exposed conducting line sidewalls;
(vi) removing the insulating layer over the HDP oxide layer using chemical mechanical polishing;
(vii) etching exposed areas of the first HDP oxide layer;
(viii) removing the insulating layer;
(ix) forming insulating spacers (20) on the upper portion of the sidewalls of the conducting lines;

(x) depositing a second HDP oxide layer (22) over the first HDP oxide layer; and

(xi) completing the **integrated circuit** device.

The isotropic etching of the first HDP exposes the upper portion of the sidewalls of the conducting lines. The deposition of the second HDP over the first HDP oxide layer fills the keyhole.

USE - For **semiconductor devices**.

ADVANTAGE - Eliminates shorting of conductive material through voids in the dielectric layer between narrowly spaced adjacent conducting lines, metal oxide **semiconductor** gates, or gaps.

DESCRIPTION OF DRAWING(S) - The drawing shows a completed **integrated circuit** device.

Substrate (10)
First HDP oxide layer (14)
Insulating spacers (20)
Second HDP oxide layer (22)
Conducting lines (30)
pp; 9 DwgNo 12/13

33/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013052591
WPI Acc No: 2000-224446/200019
XRAM Acc No: C00-068581
XRPX Acc No: N00-168174
Forming structure on substrate by depositing two dielectric layers one over the other on substrate, and etch mask having a via pattern on the top dielectric layer, for forming interconnect lines and via plugs using dual damascene techniques
Patent Assignee: APPLIED MATERIALS INC (MATE-N)
Inventor: BROYDO S; HEY H P W; NAIK M B; PARIKH S A
Number of Countries: 023 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200010202	A1	20000224	WO 99US18034	A	19990809	200019	B
EP 1110241	A1	20010627	EP 99939712	A	19990809	200137	
			WO 99US18034	A	19990809		
TW 437040	A	20010528	TW 99113498	A	19990806	200172	
KR 2001072404	A	20010731	KR 2001701776	A	20010210	200209	

Priority Applications (No Type Date): US 98133075 A 19980812
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200010202	A1	E	37	H01L-021/768	
Designated States (National): JP KR SG					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
EP 1110241	A1	E		H01L-021/768	Based on patent WO 200010202
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
TW 437040	A			H01L-023/522	
KR 2001072404	A			H01L-021/768	

Abstract (Basic): WO 200010202 A1
Abstract (Basic):
NOVELTY - Structure is formed on a substrate (310) by depositing two dielectric layers (314,316) of different etching characteristics, one over the other on the substrate. An etch mask with a via pattern is deposited on the second layer. It is anisotropically etched through the dielectric layers to form a via hole in the first layer. The etch mask is removed, and a trench is etched in the second dielectric layer.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for (A) a device comprising a substrate (310), two dielectric layers of different etching characteristics, a first region in the first dielectric layer (314) defining a via hole extending through the first layer, and a second region in the second dielectric layer (316) defining a trench on the underlying via hole, which extends through the second dielectric layer; where the via hole and the trench are adapted to contain a dual damascene structure; and (B) an apparatus for

controlling the formation of a fabricated structure on a substrate, which comprises at least one controller to interact with several fabrication stations, and a data structure which causes the controller to control the formation of the fabricated structure.

USE - The invention is used for forming **IC** structure on a substrate, for the fabrication of **semiconductor device** interconnect lines and via plugs using dual damascene techniques.

ADVANTAGE - The invented method results in additional improved damascene fabrication techniques because the via etch does not require etching of very deep vias, as compared with prior art dual damascene techniques. It avoids the use of a timed etch, resulting in improved etch depth control, and also avoids the use of an etch stop layer between the inter-metal layer and the intra-metal dielectric layers, thus facilitating fabrication and resulting in quality improvements and cost reductions. It optimizes the mechanical, thermal, and electrical properties of the structure.

DESCRIPTION OF DRAWING(S) - The figure is a schematic cross-sectional side view of the invented structure.

Substrate (310)
First dielectric layer (314)
Second dielectric layer (316)
Via plug (332)

33/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012989126
WPI Acc No: 2000-160979/200014
XRAM Acc No: C00-050358
XRPX Acc No: N00-120081
Fabrication of dual damascene structure used e.g., for **integrated circuit** by depositing two dielectric layers with an etch stop layer between them, forming hard mask layer, depositing photoresist, forming via pattern and anisotropic etching
Patent Assignee: APPLIED MATERIALS INC (MATE-N)
Inventor: PARIKH S A
Number of Countries: 023 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200003433	A1	20000120	WO 99US14926	A	19990630	200014	B
US 6127263	A	20001003	US 98113578	A	19980710	200050	
EP 1099248	A1	20010516	EP 99935388	A	19990630	200128	
			WO 99US14926	A	19990630		
KR 2001053487	A	20010625	KR 2001700432	A	20010110	200173	

Priority Applications (No Type Date): US 98113578 A 19980710
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200003433	A1	E	43	H01L-021/768	
Designated States (National): JP KR SG					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
US 6127263	A			H01L-021/4763	
EP 1099248	A1	E		H01L-021/768	Based on patent WO 200003433
Designated States (Regional): BE CH DE GB LI NL					
KR 2001053487	A			H01L-021/768	

Abstract (Basic): WO 200003433 A1
Abstract (Basic):

NOVELTY - Dual damascene structure is fabricated by depositing dielectric layers (210, 216) on the substrate (212) with an etch stop layer (214) in between; forming a hard mask layer having a trench pattern; depositing a first photoresist; forming a via pattern over the underlying trench pattern; and anisotropically etching the via pattern through the hard mask layer in the first etching procedure.

DETAILED DESCRIPTION - Dual damascene structure is fabricated by depositing a first and second dielectric layer (210, 216) on the substrate (212) with an etch stop layer (214) in between; forming a hard mask layer having a trench pattern on the second dielectric layer; depositing a first photoresist on the hard mask layer; forming a via pattern over the underlying trench pattern in the first photoresist; and anisotropically etching the via pattern through the hard mask layer in the first etching procedure. The first and second dielectric layers comprise materials of the same etching characteristics.

INDEPENDENT CLAIMS are also included for the following:

(A) a device with the fabricated dual damascene structure; and (B) an apparatus for controlling the formation of a fabricated structure on a substrate.

USE - For the fabrication of dual damascene structure useful in **semiconductor device** such as **integrated circuit** (**IC**).

ADVANTAGE - The misalignment compensating feature causes the trench and the line to be widened at the misalignment compensating segment. The width of the via plug is not reduced when the via mask and the trench mask are misaligned. Etching degradation of etch stop and photoresist layers is reduced because the trench and the via hole are formed simultaneously.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of an **IC** structure.

First dielectric layer (210)
Substrate (212)
Etch stop layer (214)
Second dielectric layer (216)
pp; 43 DwgNo 2H/7

33/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010218964
WPI Acc No: 1995-120218/199516
XRAM Acc No: C95-055332
XRPX Acc No: N95-094711
Semiconductor mfr.by forming photoresist and etching - on **aluminium-copper** and plasma silicon nitride layer and pressure polishing exposed layer
Patent Assignee: NEC CORP (NIDE)
Inventor: MURASE H
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7045616	A	19950214	JP 93207218	A	19930729	199516	B
US 5502007	A	19960326	US 94283295	A	19940728	199618	

Priority Applications (No Type Date): JP 93207218 A 19930729
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7045616	A		5	H01L-021/3205	
US 5502007	A		16	H01L-021/302	

Abstract (Basic): JP 7045616 A

The **semiconductor device** manufacturing method involves forming **aluminium copper** film (3) and a plasma SiN layer (4) on the inter layer insulating film (2) of silicon substrate (10 thereby forming the **IC**. A patterned photoresist (5) is formed and etching of SiN layer and **aluminium copper** layer is carried out.

Etching forms **aluminium** wiring (6) of small area and **aluminium** wiring (7) of big area on insulating film. A **plasma oxide** film (8) is formed on the whole surface. Pressurization polishing is carried out until the projected SiN layer is exposed. Planarisation of the oxide film is carried out. Different polishing speed is used for the oxide film and SiN layer continuously. SiN film is used as advanced polish prevention film.

ADVANTAGE - Provides perfectly flat inter-layer insulating film. Dwg.1/3

Abstract (Equivalent): US 5502007 A

A method of forming a flat surface of an insulator film of a **semiconductor device** comprises forming a first wiring film on a **semiconductor** substrate; forming a first insulator film on the first wiring film; forming a patterned resist film on the first insulator film; patterning the first insulator film to a pattern using the patterned resist film as a mask; patterning the first wiring film using the patterned first insulator film as a mask; removing the patterned resist film to produce the patterned first wiring film formed on the substrate and the patterned first insulator film formed over the patterned first wiring film, the patterned first wiring film and the patterned first insulator film having spaces formed therein; forming a second insulator film on the patterned first insulator film to fill the

spaces with the second insulator film, the first insulator film being relatively lower in polishing rate than the second insulator film, the second insulator film having a surface being uneven due to the patterned first wiring film and the patterned first insulator film; and polishing the uneven surface of the second insulator film under pressure until the first insulator film is exposed to flatten the uneven surface of the second insulator film, the spaces remaining filled with the second insulator film.

The patterned first wiring film has a first wiring region and a second wiring region, the first wiring region being relatively lower in polishing rate than the second wiring region. The patterned first insulator film acts as a polishing stopper in the second wiring region to compensate for a difference in polishing rate between the first wiring region and the second wiring region during polishing.

Dwg.2I/3

08/09/2002 09/805,027

37/3,AB/1 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04568567 JICST ACCESSION NUMBER: 00A0095517 FILE SEGMENT: JICST-E
Year 2000 the latest **semiconductor** processing technology---Technology & Equipment--The second edition chapter 6--Electrode and wiring formation technology--Sputtering equipment INOVA--Novellus Systems.
Gekkan Semiconductor World(Semiconductor World), 1999, VOL.18,NO.3, PAGE.210-211, FIG.4
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: This paper introduces sputtering equipment INOVA of Novellus Systems, Inc. This equipment is a **PVD** system corresponding to the most-advanced 0.25.MU.m and 0.18.MU.m metallization technology. In addition to **aluminum** film formation wiring, the equipment corresponds to **liner**/barrier processing of Ti/TiN, viafill flattening of **aluminum** high aspect ratio, and also to barrier (Ta/TaN)/seed (**Cu**) for **copper** wiring. The features of the equipment are ionized **PVD** source, low particle and high yield by ultra-high vacuum and ultra-clean technologies, high-density plasma pre-clean module, and low COO. This paper explains each of the features, and also explains barrier (Ta/TaN)/seed (**Cu**) and Ti/TiN **liner**/barrier processing for **copper** wiring as mass production processing technology.

37/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009602928
WPI Acc No: 1993-296476/199338
Related WPI Acc No: 1997-387767; 2000-055557
XRAM Acc No: C93-131372
XRPX Acc No: N93-228531
Refractory metal capping of metallisation lines by **PVD** and CVD - in submicron devices permits chemical-mechanical polishing without scratching or corrosion
Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: CUOMO J J; DALAL H M; JOSHI R V; HSU L L
Number of Countries: 009 Number of Patents: 024
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 561132	A1	19930922	EP 93101519	A	19930201	199338	B
JP 5343532	A	19931224	JP 9328812	A	19930218	199405	
US 5300813	A	19940405	US 92841967	A	19920226	199413	
CN 1076548	A	19930922	CN 93101333	A	19930224	199425	
US 5403779	A	19950404	US 92841967	A	19920226	199519	
			US 92928335	A	19920812		
US 5426330	A	19950620	US 92841967	A	19920226	199530	
			US 93125107	A	19930921		
US 5585673	A	19961217	US 92841967	A	19920219	199705	
			US 93125107	A	19930921		
			US 94346208	A	19941122		

Priority Applications (No Type Date): US 92841967 A 19920226; US 92928335 A 19920812; US 93125107 A 19930921; US 94346208 A 19941122; US 96753991 A 19961203; US 98113917 A 19980710; US 98113918 A 19980710; US 98113916 A 19980710
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 561132	A1	E	20	H01L-023/485	
Designated States (Regional): DE FR GB					
JP 5343532	A		12	H01L-021/90	
US 5300813	A		15	H01L-029/440	
CN 1076548	A			H01L-021/283	
US 5403779	A		17	H01L-021/44	Div ex application US 92841967
					Div ex patent US 5300813
US 5426330	A		15	H01L-029/40	Cont of application US 92841967
					Cont of patent US 5300813

Abstract (Basic): EP 561132 A
A device, having metallisation encapsulated in refractory metal, comprises a dielectric layer (11) on a substrate (10) with metallisation (16) in an opening (14) in this layer extending from a surface planar with the dielectric towards the substrate. The metallisation comprises low resistivity metal or alloy (15) having side walls which taper inwardly towards the planar surface and is encapsulated by a refractory metal or alloy.

Also claimed is a method of forming a refractory metal **liner** as above in high aspect ratio submicron holes comprising sputtering the metal through a collimator at a pressure where scattering deposition dominates and a **liner** thick enough to promote the adhesion of CVD metal is deposited.

Also claimed is a method of creating metallisation lines and vias on a substrate as above comprising sequentially depositing a first refractory metal, the low resistivity metal, and a second refractory metal over the dielectric and at the bottom of the opening and then removing all of these from above the dielectric to leave a planar dielectric with coplanar refractory metal cap.

USE/ADVANTAGE - A device and method of forming it (claimed) are provided which are useful for metal interconnects or **semiconductor** substrates and related packages, esp. submicron circuits. The method permits effective chemo-mechanical polishing and gives superior conduction lines and vias in high yields. The need for dielectric planarisation is avoided.

Dwg.1/9

Abstract (Equivalent): US 5585673 A

A device, comprises: (a) a substrate; (b) a dielectric layer positioned on the substrate; and (c) metallisation positioned in an opening in the dielectric layer extending from a surface which is planar with a surface of the dielectric layer towards the substrate.

The metallisation comprises a low resistivity metal or alloy being encapsulated by at least one refractory metal or alloy. The low resistivity metal or alloy fills a bottom portion of the opening and extends up opposing sides of the opening towards the surface which is planar with the surface of the dielectric layer and defines a cap region.

At least a portion of at least one refractory metal or alloy is positioned within the cap region above the bottom portion and between upwardly extending side portions of the low resistivity metal or alloy. At least a portion of at least one refractory metal or alloy has a surface which is planar with the dielectric layer, where the low resistivity metal or alloy comprises a binary or ternary alloy of **aluminum** or **copper**.

Dwg.7b/9

US 5426330 A

The device comprises conductors and vias formed by applying a dielectric layer over a substrate with an opening extending to the substrate. Metallisation is applied to the dielectric walls of the opening followed by a cap of refractory metal. Between the cap and the refractory is positioned an intermediate layer of e.g. titanium metal alloy.

USE/ADVANTAGE - Used for submicron circuit prod.. Low cost corrosion free devices can be produced with high yield.

Dwg.4E/9

US 5403779 A

A method of creating a **liner** in high aspect ratio, submicron holes and lines comprises sputtering refractory metal (alloy) via a collimator into high aspect ratio submission holes or lines at a pressure where scattering deposition dominates to form a conformal coating.

Deposition is continued until sufficient thickness is obtd. to

produce adhesion of the chemical vapour deposition metal which will be subsequently deposited in the **liner**.

USE/ADVANTAGE - To form conductor lines and vias on **integrated circuits**. The process provides a simple, low cost way of producing conductors free of corrosion and with good adhesion.

2b,2d,2e/9

US 5300813 A

The device comprises (a) at least one dielectric layer on a substrate, and (b) metallisation positioned in an opening in the dielectric layers and extending from a surface which is coplanar with the dielectric layer towards the substrate. The metallisation is a low resistivity metal or alloy, encapsulated by at least one refractory metal or alloy, and has sidewalls which taper inwardly towards one another towards the metallisation surface. The refractory metal or alloy is selected from Ti, W, Ta, and Cr, their alloys and their conducting oxides, nitrides and silicides, and contains a higher Si content near the surface of the metallisation than closer to the substrate. The low resistivity metal is a binary or ternary alloy of **Al** or **Cu**.

ADVANTAGE - Low-cost, corrosion-free, wear resistant, electromigration resistant, electrical conductor interconnecting circuits on a substrate on

42/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012814631
WPI Acc No: 1999-620862/199953
XRAM Acc No: C99-181336
XRPX Acc No: N99-457918
Deposition of deep submicron metallization within high aspect ratio **semiconductor** structures for use in the construction of **integrated circuits**
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: LYONS C F; SINGH B
Number of Countries: 021 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9954930	A1	19991028	WO 99US7361	A	19990401	199953	B
EP 1080494	A1	20010307	EP 99916346	A	19990401	200114	
			WO 99US7361	A	19990401		
US 6287959	B1	20010911	US 9865352	A	19980423	200154	
KR 2001042954	A	20010525	KR 2000711779	A	20001023	200168	
JP 2002512449	W	20020423	WO 99US7361	A	19990401	200243	
			JP 2000545191	A	19990401		

Priority Applications (No Type Date): US 9865352 A 19980423
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9954930	A1	E	16	H01L-021/768	
Designated States (National): JP KR					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
EP 1080494	A1	E		H01L-021/768	Based on patent WO 9954930
Designated States (Regional): DE FR GB NL					
US 6287959	B1			H01L-021/4763	
KR 2001042954	A			H01L-021/768	
JP 2002512449	W		19	H01L-021/28	Based on patent WO 9954930

Abstract (Basic): WO 9954930 A1
Abstract (Basic):
NOVELTY - Silicon oxynitride films are used both as antireflective coatings and etch stops within deep submicron metallization structures which are commonly patterned using photoresists with deep ultraviolet wavelengths prone to be reflected by metallic surfaces.
DETAILED DESCRIPTION - Depositing metal in deep submicron **semiconductor** structures comprises depositing a silicon oxynitride film over a first metallization layer, conditioning the film to deplete surface nitrogen content, patterning the first metallization layer using deep ultraviolet photolithography, etching the layer, depositing and masking a dielectric layer, etching an opening through the dielectric layer and stopping etching of the dielectric layer upon encountering silicon oxynitride film. An INDEPENDENT CLAIM is also included for a deep submicron **semiconductor integrated circuit** interconnect structure comprising a first metallization

layer patterned into an interconnect element, a silicon oxynitride film deposited over the first metallization layer, the film being partially etched and functioning as an etch stop, and a second metallization layer deposited over the partially etched film to achieve electrical contact with the first metallization layer.

USE - The method employing silicon oxynitride films both as antireflective coatings and etch stops is used for multilayer interconnect structures in high **density integrated circuit** manufacturing.

ADVANTAGE - Silicon oxynitride can be employed as an antireflective coating and an etch stop in patterning deep submicron metallization layers. It has properties compatible with deep ultraviolet photoresists used to pattern highly dense interconnect structures.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a portion of an **integrated circuit** structure.

integrated circuit structure (10)
reflective metal layer (12)
antireflective layer (14)
photoresist (16)
pp; 16 DwgNo 1/5

42/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012784744
WPI Acc No: 1999-590970/199950
XRAM Acc No: C99-172486
XRPX Acc No: N99-435927
Chemical mechanical polishing slurry not containing a film-forming agent, useful for polishing **copper**, titanium and **titanium nitride** layers used in multiple level **semiconductor integrated circuits**
Patent Assignee: CABOT CORP (CABO); CABOT MICROELECTRONICS CORP (CABO); KAUFMAN V B (KAUF-I); KISTLER R C (KIST-I); WANG S (WANG-I)
Inventor: KAUFMAN V B; KISTLER R C; WANG S
Number of Countries: 084 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9947618	A1	19990923	WO 99US5968	A	19990318	199950	B
AU 9931004	A	19991011	AU 9931004	A	19990318	200008	
EP 1064338	A1	20010103	EP 99912683	A	19990318	200102	
			WO 99US5968	A	19990318		
CN 1301288	A	20010627	CN 99806193	A	19990318	200158	
KR 2001041962	A	20010525	KR 2000710286	A	20000918	200168	
US 20010049910	A1	20011213	US 9840630	A	19980318	200204	
JP 2002506915	W	20020305	WO 99US5968	A	19990318	200220	
			JP 2000536803	A	19990318		

Priority Applications (No Type Date): US 9840630 A 19980318
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9947618	A1	E	30	C09G-001/02	

Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ UG ZW

AU 9931004	A		C09G-001/02	Based on patent WO 9947618
EP 1064338	A1	E	C09G-001/02	Based on patent WO 9947618

Designated States (Regional): BE CH DE FR GB IE IT LI NL SE

CN 1301288	A		C09G-001/02	
KR 2001041962	A		C09G-001/02	
US 20010049910	A1		C09G-001/00	
JP 2002506915	W	31	C09K-003/14	Based on patent WO 9947618

Abstract (Basic): WO 9947618 A1
Abstract (Basic):
NOVELTY - A chemical mechanical polishing (CMP) slurry which does not contain a film-forming agent and has a pH of 5-9, comprising:
(a) an abrasive;
(b) oxidizer(s) and
(c) 0.1-5 wt.% complexing agent comprising citric, lactic,

tartaric, malonic, succinic, oxalic or amino acids and/or salts.

DETAILED DESCRIPTION - Also claimed are:

(A) A method of polishing a substrate, comprising:

(a) preparing a CMP slurry;

(b) adjusting the pH of the slurry;

(c) applying the slurry to the substrate; and

(d) removing at least a portion of the metal layer from the substrate by bringing a pad into contact with the substrate and moving the pad in relation to the substrate; and

(B) A multi-package system useful for preparing a CMP slurry, comprising:

(a) a first container containing the complexing agent;

(b) a second container containing the oxidizing agent; and

(c) the abrasive placed in either the first container, the second container or a third container.

USE - The CMP slurry is useful for polishing layers containing **copper** alloy, titanium and **titanium nitride**, and passivation layers, especially the metal layers and thin films used in multiple level, silicon **semiconductor integrated circuit** and wafers manufacture. Other substrates which can be polished include layers of pure **copper**, **copper aluminum** alloys, **titanium/titanium nitride/copper**, and **tantalum/tantalum nitride/copper** multi-layer substrates, and **PVD copper** wafers. The method can also be used in the production of metallized vias in insulator films and **interlayer** dielectrics for the formation of interconnection lines.

ADVANTAGE - The new CMP slurry compositions are capable of polishing at high rates while exhibiting good selectivity towards dielectric layers. Polishing can be performed at a controlled rate by forming a reproducibly thin passivating layer, to give more consistent and controllable results. **Copper** removal rates of 807-2396 Angstrom/minute, tantalum removal rates of 408-434 Angstrom/minute and PETEOS removal rates of 135-77 Angstrom/minute are obtained (in examples). By using a complexing agent, the passivation ability of the oxidizer is not significantly affected, and a film forming agent is not needed to limit **copper** corrosion rates. The shelf life of the CMP product is also increased.

pp; 30 DwgNo 0/0

42/3,AB/3 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

03750126
LIQUID CRYSTAL DISPLAY DEVICE

PUB. NO.: 04-115226 [JP 4115226 A]
PUBLISHED: April 16, 1992 (19920416)
INVENTOR(s): FUJIMORI KEITARO
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-234719 [JP 90234719]
FILED: September 05, 1990 (19900905)
JOURNAL: Section: P, Section No. 1398, Vol. 16, No. 368, Pg. 165, August 07, 1992 (19920807)

ABSTRACT

PURPOSE: To obtain a small-sized, high-reflectivity active matrix display panel by flattening the surface of a reflecting layer formed covering a picture element transistor(TR) by a mechanical grinding after a reflecting layer constitution material is deposited.

CONSTITUTION: An **inter-layer** insulating film 8 is formed and after a contact hole 24 is bored, an electrode material and light reflecting material is deposited by sputtering or **vapor deposition. Aluminum**, **aluminum** silicon, **aluminum** silicon **copper** , gold, and other metals are usable as the material. In the manufacture process of a **semiconductor integrated circuit**, **vapor deposition** is carried out for metal wiring to an about 20,000 - 50,000 angstroms film thickness. At this time, the material is deposited without raising the temperature so that fine crystal is not grown. Then a specular surface is formed by mechanical grinding and the film thickness of the reflecting film is reduced finally to about 15,000 angstroms . Then the surface where the active element of the **semiconductor integrated circuit** is formed is mechanically ground after the active element is formed. Consequently, a surface with a high optical reflection factor is obtained without exerting any influence upon the active element according to the material and formation conditions, etc., of the reflecting film.

47/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013595400
WPI Acc No: 2001-079607/200109
XRAM Acc No: C01-022816
XRPX Acc No: N01-060570
Fabrication of hybrid, low-dielectric constant intermetal dielectric layer for multilevel metal **interconnections** on **integrated circuits**, involves using low-dielectric constant porous materials
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: CHANG W; CHENG Y
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6159842	A	20001212	US 99229382	A	19990111	200109	B

Priority Applications (No Type Date): US 99229382 A 19990111
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6159842	A		7	H01L-021/00	

Abstract (Basic): US 6159842 A
Abstract (Basic):
NOVELTY - A hybrid low-dielectric constant (low-k) intermetal dielectric (IMD) layer is fabricated by depositing and patterning a conductive layer; depositing a conformal insulating layer, and a porous first low-k material; etching and plasma treating the porous first low-k material; and depositing a denser second low-k material.
DETAILED DESCRIPTION - Fabrication of hybrid low-k IMD layer comprises providing a **semiconductor** substrate (10) having **semiconductor devices** and an insulating layer (12); depositing a conductive layer (14) on the insulating layer; patterning the conductive layer to form electrical **interconnecting** lines to contact the devices; depositing a conformal insulating layer (16) as a protective layer over the patterned conductive layer; depositing a porous first low-k material (18) over the insulating layer to provide a material having minimum k between the **interconnecting** lines; etching back the porous first low-k material to the conformal insulating layer and leaving portions of the first low-k material in spaces between the **interconnecting** lines to minimize intralevel capacitance; plasma treating the porous first low-k material to densify the surface; and depositing a denser second low-k material (20) over the electrical **interconnecting** lines and the porous first low-k material to form a cap layer which protects the first low-k material and to minimize interlevel capacitance and complete the hybrid low-k IMD layer.
USE - For fabricating hybrid low-k IMD layer for multilevel metal **interconnections** on **integrated circuits**.
ADVANTAGE - The low-k IMD reduces the RC time constant, thus increasing the performance of the circuit since the **signal propagation** time in the circuit is inversely affected by the RC

delay time, where R is the resistance of the metal line, and C is the inter- or intralevel capacitance.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic sectional view of the hybrid low-k IMD layer.

Substrate (10)
Insulating layer (12)
Conductive layer (14)
Conformal insulating layer (16)
First low-k material layer (18)
Second low-k material layer (20)
pp; 7 DwgNo 2/3

52/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014261232
WPI Acc No: 2002-081930/200211
XRAM Acc No: C02-024683
XRPX Acc No: N02-060988

Formation of electrically conductive material layer on spaced apart recesses involves forming overburden layer of electrically conductive material, and chemical-mechanical polishing exposed upper surface of the layer

Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: AVANZINO S C; ERB D M; WANG F

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6319834	B1	20011120	US 99149439	P	19990818	200211	B
			US 2000639812	A	20000817		

Priority Applications (No Type Date): US 99149439 P 19990818; US 2000639812 A 20000817
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6319834	B1		10	H01L-021/44	Provisional application US 99149439

Abstract (Basic): US 6319834 B1
Abstract (Basic):

NOVELTY - A layer of electrically conductive material filling spaced-apart recesses is formed by performing a plating process for forming a predetermined thickness overburden layer of an electrically conductive material over an upper surface of the substrate; and chemical-mechanical polishing of the exposed upper surface of the overburden layer.

DETAILED DESCRIPTION - Formation of a layer of electrically conductive material filling spaced-apart recesses of different widths and depths in a substrate (1) surface involves:

(a) providing a substrate with an exposed upper surface having spaced-apart recesses of different depths, and non-recessed areas (4) in between;

(b) performing a first, selective plating process for selectively filling the recesses with the electrically conductive material while leaving the non-recessed areas unplated;

(c) performing a second plating process for forming a predetermined thickness overburden layer (5) of the electrically conductive material over the upper surface of the substrate; and

(d) chemical-mechanical polishing (CMP) of the exposed upper surface of the overburden layer. The polishing is carried out to remove the portions covering the non-recessed areas of the upper surface of the substrate, and to render the exposed upper surfaces of the portions of the electrically conductive material filling the recesses co-planar with the non-recessed areas of the upper surface of the substrate. The recesses have wide and narrow recesses. The exposed upper surface of

the overburden layer is planar.

USE - The method is used for forming electrically conductive material layer during the formation of **semiconductor integrated circuit** devices.

ADVANTAGE - The method is carried at a lower cost with higher manufacturing throughput than that of prior art. It uses **copper** -based back-end contacts and **interconnections** by a damascene process, with greater uniformity and planarity and reduced defects. It has increased speed, lower cost and greater uniformity and planarity than conventional electroplating and CMP-based processes. It is fully compatible with existing process. Processing time interval is reduced, due to reduced thickness of **copper** overburden layer to be removed by the CMP, thus decreasing the manufacturing costs.

DESCRIPTION OF DRAWING(S) - The figure shows a sequence of steps for performing the inventive damascene-type metallization process, in a simplified cross-sectional form.

Substrate (1)
Non-recessed areas (4)
Overburden layer (5)
pp; 10 DwgNo 3/5

52/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014189771
WPI Acc No: 2002-010468/200201
XRAM Acc No: C02-002469
XRPX Acc No: N02-008787
Formation of dielectric layer for microelectronic device production, involves application of electron beam to chemical **vapor deposited** material
Patent Assignee: ELECTRON VISION CORP (ELEC-N)
Inventor: ROSS M F; THOMPSON H; YANG J
Number of Countries: 022 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200161737	A1	20010823	WO 2001US3440	A	20010202	200201	B

Priority Applications (No Type Date): US 2000506515 A 20000217
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200161737	A1	E	30	H01L-021/3105	

Designated States (National): CA JP KR
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR

Abstract (Basic): WO 200161737 A1
Abstract (Basic):
NOVELTY - Reduction of the dielectric constant of chemical **vapor deposited** films which are useful for the production of microelectronic devices.
DETAILED DESCRIPTION - A dielectric layer is formed on a substrate by chemical **vapor depositing** a monomeric or oligomeric dielectric precursor in a chemical **vapor deposition** apparatus or a reaction product formed from the precursor into a substrate to form a layer on the substrate surface, optionally heating the layer, and exposing the layer to electron beam radiation.
USE - For forming dielectric layer useful for the production of microelectronic devices (claimed), silicon chips, **integrated circuits**, and for **interconnect** applications.
ADVANTAGE - The invention provides reduced dielectric constant of chemical **vapor deposited** films, thus providing a cost advantage to device manufacturers because they can extend their existing equipment with minimal cost. It achieves the reduction in both peak process temperature and total process time.
pp; 30 DwgNo 0/0

52/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014080167
WPI Acc No: 2001-564381/200163
XRAM Acc No: C01-167475
XRPX Acc No: N01-420101
Formation of damascene structure involves defining via pattern and **interconnect** line pattern in second etch stop layer and etching via pattern through second dielectric layer and through second stop layer
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: CHENG C; HSU K; LIU M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6284642	B1	20010904	US 99372077	A	19990811	200163	B

Priority Applications (No Type Date): US 99372077 A 19990811
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6284642	B1		9	H01L-021/4763	

Abstract (Basic): US 6284642 B1
Abstract (Basic):

NOVELTY - Forming a damascene structure over a **semiconductor** surface comprises defining a via pattern and **interconnect** line pattern in second etch stop layer and performing a first etch to etch the via pattern through second dielectric layer and through second etch stop layer.

DETAILED DESCRIPTION - Forming a damascene structure over a **semiconductor** surface comprises providing a **semiconductor** substrate (10) having points of electrical **interconnect** in or on its surface and sequentially depositing a first dielectric layer (12), a first etch stop layer (14), a second dielectric layer (16), and a second etch stop layer (18). The second etch stop layer is patterned and etched to create a via pattern having a via width through the second etch stop layer. An etch-resistant material layer (22) is patterned and etched over the surface of the second etch stop layer to create an opening (24) in the layer of etch stop material that aligns with the via pattern having an **interconnect** line width. At least one opening (26) having an **interconnect** line width in the layer of etch-resistant material that does not align with the via pattern is also created. A first etch is performed extending the width of the via pattern in the second etch stop layer to a width of an **interconnect** line pattern. The first etch etches the via pattern in the second etch stop layer through the second layer of dielectric, through the first etch stop layer and partially into the first layer of dielectric. The first etch further etches the second etch stop layer in accordance with the opening(s) not aligned with the via pattern. A second etch is performed. The via partially etched into the first layer of dielectric is further etched through the first layer of dielectric down to the substrate surface. The second etch further etches the

interconnect line pattern through the second layer of dielectric and partially through the first etch stop layer to complete the creation of a damascene structure. The second etch further etches the second layer of dielectric in accordance with the opening(s) not aligned with the via pattern.

USE - For forming a damascene structure over a **semiconductor** surface in the fabrication of **integrated circuit** devices.

ADVANTAGE - The method uses only one etch processing step to create the desired vias and **interconnect** line pattern. The use of the second stop layer to define the via offers improved photolithographic overlay and etching control since it eliminates problems of misalignment between the **interconnect** line pattern and the via layer.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of the deposited layers after the first etch.

Substrate (10)
First dielectric layer (12)
First etch stop layer (14)
Second dielectric layer (16)
Second etch stop layer (18)
Etch-resistant material layer (22)
Opening (24, 26)
pp; 9 DwgNo 3/6

52/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013904301
WPI Acc No: 2001-388514/200141
XRAM Acc No: C01-118483
XRPX Acc No: N01-285615
Formation of **interconnect** by forming barrier layer over dielectric layer, forming trench, depositing **copper** on barrier layer, planarizing **copper** and barrier layers, and depositing **copper** on dished **copper** filled trench
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: LIU C; YU C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6225223	B1	20010501	US 99374297	A	19990816	200141	B

Priority Applications (No Type Date): US 99374297 A 19990816
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6225223	B1		5	H01L-021/44	

Abstract (Basic): US 6225223 B1
Abstract (Basic):
NOVELTY - An **interconnect** is formed by forming a barrier layer over a dielectric layer on top of the **semiconductor** substrate, lining trench side walls and bottom; depositing **copper** on the barrier layer; planarizing the first **copper** layer and the barrier layer; selectively depositing **copper** on the dished **copper** filled trench to form a second **copper** layer over the dished **copper** filled trench.
DETAILED DESCRIPTION - An **interconnect** is formed by (a) providing a **semiconductor** structure (10); b) forming a dielectric layer (11), over the **semiconductor** structure, having an upper surface; (c) forming a trench, within the dielectric layer, having side walls and a bottom; (d) forming a barrier layer (16) over the dielectric layer and lining the trench side walls and bottom; (e) depositing **copper** on the barrier layer to form a first **copper** layer (12) filling the lined trench and blanket filling the barrier layer covered dielectric layer; (f) planarizing the first **copper** layer and the barrier layer on the upper surface of the dielectric layer, exposing the upper surface of the dielectric layer and forming a dished **copper** filled trench; and (g) selectively depositing **copper** on the dished **copper** filled trench to form a second **copper** layer over the dished **copper** filled trench and extending above the upper surface of the dielectric layer.
USE - For forming **copper interconnects** in microminiaturized **integrated circuits** in **semiconductor devices**.
ADVANTAGE - The formation of a planarized **copper interconnect** allows for well-controlled **copper** resistance

distribution and facilitates well-controlled photo, etching, thin film chemical mechanical processes.

DESCRIPTION OF DRAWING(S) - The figure shows the **copper interconnect** structure.

Semiconductor structure (10)
Dielectric layer (11)
First **copper** layer (12)
Barrier layer (16)
pp; 5 DwgNo 4/4

52/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013474531
WPI Acc No: 2000-646474/200062
XRAM Acc No: C00-195446
XRPX Acc No: N00-479069

Formation of electrically conductive material layer filling high aspect ratio recess(es) in workpiece surface involves filling with electrically conductive material layer by electroplating

Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: AVANZINO S C; LUKANC T P; WANG F
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6117782	A	20000912	US 99296556	A	19990422	200062	B

Priority Applications (No Type Date): US 99296556 A 19990422
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6117782	A		14	H01L-021/00	

Abstract (Basic): US 6117782 A
Abstract (Basic):

NOVELTY - A layer of an electrically conductive material filling high aspect ratio recess(es) formed in a workpiece surface is formed by making dual-layered dielectric layer, filling the recess with an electrically conductive material layer by electroplating the layer on conductive nucleation/seed layer on recess surface portions, and planarizing the recess-filled surface.

DETAILED DESCRIPTION - A layer of an electrically conductive material filling at least one high aspect ratio recess (2) formed in a workpiece (10) surface is formed by making a dielectric layer on the substrate (1) surface. The dielectric layer (3) comprises lower (3L) and upper portions of dielectric materials in contact with the substrate. At least one high aspect ratio recess is formed in a surface of the dielectric layer by two-stage etching. The recess comprises: a mouth surface portion at the upper end formed by a first etching and having an opening with a width profile tapering from a wider width at the dielectric layer surface (11) to a second, narrower width at a first depth below the dielectric surface equal to the second thickness of the upper portion of the dielectric; an interior wall surface portion of the second, narrower width formed by a second etching process extending at a constant width from the first depth to the second depth below the dielectric surface and terminating within the lower portion of the dielectric; and a bottom surface portion at the second depth.

The mouth portion borders an adjacent, non-recessed portion of the dielectric surface. An electrically conductive nucleation/seed layer (7, 8) is formed on the recess surface portions where formation of overhanging portions of the layer at the mouth surface is prevented due to the wider width of the recess at the dielectric surface and inwardly

tapered width profile. The recess is filled with a layer of an electrically conductive material (5') by electroplating the layer on the nucleation/seed layer. At least one of occlusion and pinching off of the recess mouth surface during the electroplating due to formation of overhanging portions of the conductive material layer on overhanging portions of the nucleation/seed layer is prevented. The recess-filled surface (6) is planarized by removing the entire second thickness of the upper portion of the dielectric material, thus removing mouth portion from the filled recess.

An INDEPENDENT CLAIM is also included for an **integrated circuit semiconductor device** formed by the method.

USE - The method is used for forming a layer of an electrically conductive material filling high aspect ratio recess(es) formed in a substrate surface.

ADVANTAGE - The method enables the formation of extremely reliable **interconnect** members and patterns, e.g. **copper** or its alloy having high reliability, high yield, high performance, and reduced incidence of defects, e.g. voids. It reduces time and cost of back end damascene-type processing.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional form of the workpiece after planarization.

Substrate (1)
High aspect ratio recess (2)
Dielectric layer (3)
Lower portion (3L)
Electrically conductive material (5')
Recess-filled surface (6)
Nucleation/seed layer (7, 8)
Workpiece (10)
Dielectric layer surface (11)
pp; 14 DwgNo 6/6

52/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013474530
WPI Acc No: 2000-646473/200062
XRAM Acc No: C00-195445
XRPX Acc No: N00-479068
Formation of electrically conductive material layer filling high aspect ratio recess(es) in substrate surface involves filling with electrically conductive material layer by electroplating
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: AVANZINO S C; LUKANC T P; WANG F
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6117781	A	20000912	US 99296553	A	19990422	200062	B

Priority Applications (No Type Date): US 99296553 A 19990422
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6117781	A		13	H01L-021/00	

Abstract (Basic): US 6117781 A
Abstract (Basic):
NOVELTY - A layer of an electrically conductive material filling high aspect ratio recess(es) in a substrate surface is formed by filling the recess with an electrically conductive material layer, by electroplating the layer on conductive nucleation/seed layer on recess surface portions.

DETAILED DESCRIPTION - A layer of an electrically conductive material filling at least one high aspect ratio recess (2) in a substrate (1) surface is formed by making high aspect ratio recess(es) in a surface of the substrate. The recess comprises: a mouth surface portion at its upper end having an opening with a width profile at the substrate surface to a second, narrower width at a first depth below the substrate surface; an interior wall surface portion of the second, narrower width extending at a constant width from the depths below the substrate surface; and a bottom surface portion at the second depth. An electrically conductive nucleation/seed layer (8) is formed on the recess surface portions. Formation of overhanging portions of the layer at the mouth surface is prevented due to the inwardly tapered width profile. The recess is filled with a layer of an electrically conductive material (5) by electroplating the layer on the nucleation/seed layer. At least one of occlusion and pinching off of the recess mouth surface during the electroplating due to formation of overhanging portions of the conductive material layer on overhanging portions of the nucleation/seed layer is prevented.

An INDEPENDENT CLAIM is also included for an **integrated circuit semiconductor device** produced by the method.

USE - The method is used for forming a layer of an electrically conductive material filling high aspect ratio recess(es) formed in a substrate surface.

ADVANTAGE - The method enables the formation of extremely reliable **interconnect** members and patterns, e.g. **copper** or its alloy having high reliability, high yield, high performance, and reduced incidence of defects, e.g. voids. It reduces time and cost of back end damascene-type processing.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional form of the workpiece after electroplating.

Substrate (1)
High aspect ratio recess (2)
Dielectric layer (3)
Layer of an electrically conductive material (5)
Adhesion promoting/diffusion barrier layer (7)
Electrically conductive nucleation/seed layer (8)
pp; 13 DwgNo 7/7

52/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012975836
WPI Acc No: 2000-147685/200013
XRAM Acc No: C00-046355
XRPX Acc No: N00-109279
Forming a **copper** film with good adhesion on a substrate for **semiconductor integrated circuit interconnects**, e.g. inlaid **copper** metal lines and plugs
Patent Assignee: CVC INC (CVCC-N); CAMPBELL D R (CAMP-I); LIU Z (LIUZ-I); MOSLEHI M M (MOSL-I); OMSTEAD T R (OMST-I); PARANJPE A P (PARA-I); SHANG G (SHAN-I); VELO L A (VELO-I)
Inventor: CAMPBELL D R; LIU Z; MOSLEHI M M; OMSTEAD T R; PARANJPE A P; SHANG G; VELO L A
Number of Countries: 087 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200003420	A2	20000120	WO 99US15583	A	19990709	200013	B
AU 9949817	A	20000201	AU 9949817	A	19990709	200028	
EP 1108266	A2	20010620	EP 99933852	A	19990709	200135	
			WO 99US15583	A	19990709		
US 20020006468	A1	20020117	US 98113852	A	19980710	200212	

Priority Applications (No Type Date): US 98113852 A 19980710
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200003420	A2	E	38	H01L-021/00	

Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ UG ZW

AU 9949817	A		H01L-021/00	Based on patent WO 200003420
EP 1108266	A2	E	H01L-021/285	Based on patent WO 200003420

Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

US 20020006468	A1		B05D-005/12

Abstract (Basic): WO 200003420 A2
Abstract (Basic):
NOVELTY - **Copper** film is formed on a substrate by depositing a seed layer on the substrate according to first predetermined conditions and depositing a **copper** layer over it through second predetermined conditions including chemical **vapor deposition** (CVD). The predetermined conditions are adhesion promotion techniques that repair the interface of the **copper** film and the substrate.
USE - For forming **semiconductor integrated circuit interconnects**, e.g. inlaid **copper** metal lines and plugs. It is particularly for forming a **copper interconnect** on a substrate diffusion barrier (claimed).

ADVANTAGE - New method deposits a seed layer that has a good adhesion with the underlying layer of the substrate. A bulk layer of **copper** can then be deposited on the seed layer to ensure that the **copper interconnect** will maintain good adhesion throughout an entire process of **semiconductor** chip fabrication. This leads to less complex fabrication process and types of equipment required to deposit the **copper** layer film. Reaction chambers required for promoting **copper** layer adhesion are compatible with vacuum-integrated cluster equipment leading into a simpler and more reliable deposition process. The method increases the commercial production of **semiconductor** chips. It is also scalable to small feature sizes of high aspect ratio structures that are commonly encountered in advanced **interconnects**.

pp; 38 DwgNo 0/6

57/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014268459
WPI Acc No: 2002-089157/200212
XRAM Acc No: C02-027384
XRPX Acc No: N02-065689
Formation of intermetal protective layer between metallurgy lines on **semiconductor** surface, involves encapsulating substrate with passivation layer using high density plasma-chemical **vapor deposition**
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: CHIEN H; DUN J; TSAI C C; WANG Y
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010030351	A1	20011018	US 99418032	A	19991014	200212 B
			US 2001882678	A	20010618	

Priority Applications (No Type Date): US 99418032 A 19991014; US 2001882678 A 20010618
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010030351	A1		9	H01L-029/00	Div ex application US 99418032 Div ex patent US 6268274

Abstract (Basic): US 20010030351 A1
Abstract (Basic):

NOVELTY - An intermetal protective layer is formed between metallurgy lines on a **semiconductor** surface, by encapsulating a **semiconductor** substrate with first passivation layer by high density plasma-chemical **vapor deposition** (HDP-CVD). Encapsulation is stopped, and an inert gas is impinged to the backside of the substrate. Encapsulation is resumed to generate a second passivation layer.

DETAILED DESCRIPTION - Formation of an intermetal protective layer between closely spaced metallurgy lines on a **semiconductor** surface comprises encapsulating a **semiconductor** substrate with a first passivation layer. The first passivation layer is formed by high density plasma-chemical **vapor deposition** (HDP-CVD). The encapsulating process is stopped, and an inert gas is impinged to the backside of the substrate for cooling the passivation layer and the metallurgy lines. The encapsulation process is resumed on the first protective layer, to generate a second passivation layer.

An INDEPENDENT CLAIM a **semiconductor** wafer having metal circuitry comprising a silicon wafer having an upper lateral surface; individual metal circuitry disposed on the upper lateral surface; a first dielectric layer covering the individual metal circuitry lines and areas of uncovered the silicon wafer upper lateral surface, the first dielectric layer applied by HDP-CVD with a D/S ratio of 3-5 and is 5000Angstrom thick; and second dielectric layer covering the first dielectric, the second dielectric layers applied by HDP-CVD with a D/S

ratio of 5-7 and are 5000Angstrom thick.

USE - For the formation on intermetal protective layer for **integrated circuits interconnecting** active and passive elements.

ADVANTAGE - The method reduces the damage such as metal distortion to conductive lines caused by HDP-CVD of silicon oxide insulating layers.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross sectional view of the **semiconductor** wafer.

pp; 9 DwgNo 1/2

57/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013796846
WPI Acc No: 2001-281058/200129
Related WPI Acc No: 2000-085653
XRAM Acc No: C01-085364
XRPX Acc No: N01-200389

Chemical mechanical polishing for planarizing device wafers comprises providing insulating layer on wafer with non-planar surface topography, chemical-mechanical polishing insulating layer and depositing another polysilicon layer

Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: LIANG M; SU C; WANG C; WUU S

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6218286	B1	20010417	US 96682457	A	19960717	200129	B
			US 99395286	A	19990913		

Priority Applications (No Type Date): US 96682457 A 19960717; US 99395286 A 19990913
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6218286	B1		6	H01L-021/4763	Div ex application US 96682457 Div ex patent US 6001731

Abstract (Basic): US 6218286 B1
Abstract (Basic):

NOVELTY - Chemical mechanical polishing comprises: providing an insulating layer of a first thickness over a device wafer with non-planar surface topography; chemical-mechanical polishing the insulating layer; and depositing another polysilicon layer to prevent barely exposed or exposed underlying polysilicon from shorting to the next polysilicon or metal level of **interconnects**.

DETAILED DESCRIPTION - Method for making multi-level metallurgical **interconnect** on a metal oxide **semiconductor** field effect transistor (MOSFET) circuit comprises:

(a) providing a dielectric layer over conductive regions of the MOSFET circuit;

(b) photolithographic processing to open contact openings in the photoresist layer overlying the dielectric layer, and exposing the underlying dielectric layer, directly over the conductive regions of the MOSFET device's source, drain and gate polysilicon;

(c) anisotropic etching of the dielectric layer, in the contact opening of the photoresist to form contact opening to the underlying conductive regions of the MOSFET device;

(d) removing the photoresist and surface cleaning the underlying conductive region in the contact hole;

(e) depositing a titanium layer on the surface of the dielectric layer, and in the lining of the contact hole including the exposed surface of the underlying conductive region at the bottom of the

contact hole;
(f) depositing a **titanium nitride** layer on the titanium layer;
(g) depositing a tungsten layer on the **titanium nitride** layer, forming a tungsten plug in the contact hole by completely filling the contact opening;
(h) depositing an **aluminum** based **interconnect** metallization layer on the tungsten layer and over the tungsten plug in the contact hole;
(i) depositing an insulating layer for planarization of non-planar topographic surface;
(j) planarizing the non-planar topographic surface by chemical-mechanical polishing (CMP);
(k) depositing an additional insulating layer, following the polishing process, over the planarized surface to cover the underlying high topographic area, where the insulating layer becomes either very thin over the **aluminum** based metal wiring or the metal is exposed; and
(l) depositing a subsequent level of metal **interconnect** runners.
USE - Chemical mechanical polishing process is used for planarizing device wafers having multiple levels of polysilicon layers sandwiched between insulating layers. The multilevel **interconnect** is used in static-random access memory (SRAM), or other metal-oxide-silicon (MOS) or complementary metal-oxide-silicon (CMOS) circuits.
ADVANTAGE - Chemical mechanical polishing planarization process prevents multi-polysilicon and multi-metal level electrical shorts.
DESCRIPTION OF DRAWING(S) - The drawings show a schematic cross section of the **semiconductor integrated circuit** device at a subsequent stage of processing and a schematic cross section of the **semiconductor integrated circuit** device at high topographic site on the wafer, after planarization processing with chemical-mechanical polishing.
Thick field oxide regions (21)
Oxide insulating sidewall spacer (22)
Self-aligned contact polysilicon (23)
Source region (24)
Drain region (25)
Polysilicon gate structure (26)
Silicon oxide layer (27)
TEOS oxide (28)
Polished surface (29)
pp; 6 DwgNo 2, 3A/4

57/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013617503
WPI Acc No: 2001-101711/200111
Related WPI Acc No: 2002-314607
XRAM Acc No: C01-029610
XRPX Acc No: N01-075472

Making of polysilicon resistors for **integrated circuits** on a substrate, involves forming a metal silicide layer on a patterned polysilicon layer with contacts extending over the metal silicide layer

Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: HSU Y; LIU R; TSAI J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6165861	A	20001226	US 98152348	A	19980914	200111	B

Priority Applications (No Type Date): US 98152348 A 19980914
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6165861	A		8	H01L-021/20	

Abstract (Basic): US 6165861 A
Abstract (Basic):

NOVELTY - Polysilicon resistors are made on a substrate by forming a patterned polysilicon layer having two ends on the field oxide regions of a substrate, conductively doping the patterned layer to form resistors, and forming a metal silicide layer over and on the first end of the patterned layer. The patterned metal layer extends over the patterned polysilicon layer.

DETAILED DESCRIPTION - Making polysilicon resistors on a substrate comprises (i) providing a substrate (10) with field oxide (12) regions on the surface; (ii) forming a patterned polysilicon layer having two ends on the field oxide regions; (iii) conductively doping the patterned layer to a predetermined concentration to form resistors (16B); (iv) forming a metal silicide layer (20) over and on the first end of the patterned layer; (v) depositing an interlevel dielectric layer (ILD) over the patterned layer; (vi) forming contact holes (23) in the ILD to the two ends of the patterned layer, the holes to the first end are over and to the metal silicide layer; and (vii) depositing a metal layer (26) and patterning to form **interconnections** and to make first and second metal plugs (24) to the second ends. The patterned metal layer extends over the patterned polysilicon layer to prevent hydrogen from diffusing through the ILD and into the patterned polysilicon layer. The patterned metal layer have spaces (S) between the first and second contacts extending over the metal silicide layer. The metal silicide layer provides further protection from the hydrogen diffusion.

USE - For making stable, high-value polysilicon resistors and field effect transistors for **integrated circuits** on **semiconductor** substrates.

ADVANTAGE - The invention provides more stable high value resistors with spacing between the metal **interconnections** to the metal plugs aligned over the silicide layer, providing 100% metal shielding that prevents hydrogen ions from permeating the resistor.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-sectional view of the inventive polysilicon resistor integrated with a polycide gate electrode field effect transistor.

Substrate (10)
Field oxide (12)
Resistors (16B)
Metal silicide layer (20)
Contact holes (23)
Metal plugs (24)
Metal layer (26)
Spacing (S)
pp; 8 DwgNo 7/7

57/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013595398
WPI Acc No: 2001-079605/200109
XRAM Acc No: C01-022814
XRPX Acc No: N01-060568

Production of polysilicon and metal landing plugs involves forming **interconnecting** lines, forming polysilicon and metal landing plugs, and completing the landing plugs and the electrical **interconnections**

Patent Assignee: VANGUARD INT SEMICONDUCTOR CORP (VANG-N)
Inventor: CHEN B; HSIEH C; JENG E S

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6159839	A	20001212	US 99247977	A	19990211	200109	B

Priority Applications (No Type Date): US 99247977 A 19990211
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6159839	A		12	H01L-021/4763	

Abstract (Basic): US 6159839 A
Abstract (Basic):

NOVELTY - Polysilicon and metal landing plugs are produced by patterning layers of a second etch-stop, a metal, a barrier, and a polysilicon to form **interconnecting** lines, forming N+ doped polysilicon landing plugs in and metal landing plugs to N+ and P+ contact regions in device areas of first and second types, respectively, and completing the landing plugs, and the electrical **interconnections**.

DETAILED DESCRIPTION - Production of polysilicon and metal landing plugs with electrical **interconnections** for contacts on **semiconductor integrated circuits**, includes providing a **semiconductor** substrate (10) having device areas of first and second types, and having devices with N- doped contacts in the device areas of a first type, and having N+ and P+ doped contacts in the device areas of a second type. A conformal first etch-stop layer is deposited and partially etched to form sidewall spacers on the devices and to protect the device areas. An insulating layer which is planarized is deposited. First contact openings are etched in the insulating layer to the first etch-stop layer over the N- doped contacts in the device areas of a first type. The first etch-stop layer is selectively removed in the first contact openings which are self-aligned to the device to expose the N- doped contacts. An N- doped polysilicon layer is deposited on the substrate and is contacted with the N- doped contacts. Second openings in the polysilicon layer (26) and the insulating layer are etched to the first etch-stop layer over the N+ and P+ contact regions (19) in the device areas of a second type. The first etch-stop layer in the second openings is selectively etched to expose the N+ and the P+ contact regions. An electrically

conducting barrier layer is deposited. A metal layer is deposited over the thick barrier layer to fill the first and second openings and to provide a planar surface. A second etch-stop layer is deposited. The second etch-stop layer, the metal layer, the barrier layer, and the polysilicon layer are patterned to form **interconnecting** lines (32A), and concurrently to form N+ doped polysilicon landing plugs (32C) in the device areas of a first type. The metal landing plugs (42) are formed to the N+ and P+ contact regions in the device areas of a second type. The polysilicon landing plugs, the metal landing plugs, and the electrical **interconnections** are completed.

USE - For making polysilicon and metal landing plugs with electrical **interconnections** for contacts on **semiconductor integrated circuits**.

ADVANTAGE - The invention prevents over-etching the contact in the substrate and etching into the gate electrodes. It also reduces the aspect ratio of the via holes, thus making it easier to etch submicron-wide via holes.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-sectional view of a part of multilevel **interconnections**.

Via holes (8)
Substrate (10)
N+ and P+ contact regions (19)
N+ doped polysilicon layer (16A)
Insulating layer (22, 40)
Polysilicon layer (26)
Interconnecting lines (32A)
Polysilicon landing plugs (32C)
Metal landing plugs (42)
Titanium/titanium nitride (44A)
Aluminum/copper alloy (44B)
Titanium nitride (44C)
pp; 12 DwgNo 12/12

57/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013576086
WPI Acc No: 2001-060293/200107
XRAM Acc No: C01-016652
XRPX Acc No: N01-045100

Production of intermetal dielectrics on **semiconductor integrated circuits** for insulating multilevel metal **interconnections** involves using low dielectric constant spin-on polymers

Patent Assignee: IND TECHNOLOGY RES INST (INTE-N)
Inventor: KANG T; WANG C; YANG T

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6162583	A	20001219	US 9844783	A	19980320	200107	B

Priority Applications (No Type Date): US 9844783 A 19980320
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6162583	A		11	G03F-007/26	

Abstract (Basic): US 6162583 A
Abstract (Basic):

NOVELTY - Intermetal dielectrics are formed on **integrated circuits** using low dielectric constant (low k) spin-on polymers without via hole poisoning.

DETAILED DESCRIPTION - An intermetal dielectric layer is formed by:

(a) providing a **semiconductor** substrate having **semiconductor devices** protected by a first insulating layer;

(b) depositing a 1000-8000 Angstrom thick conductive layer composed of **Al/Cu** alloy having a lower barrier layer of **Ti/Ti nitride**, for contacting regions of the devices;

(c) patterning the conductive layer to form a patterned conductive layer for **interconnections** for the devices;

(d) depositing a 500-2000 Angstrom thick adhesion layer of plasma-enhanced chemical **vapor-deposited** silicon oxide on the patterned conductive layer;

(e) depositing a first 1000-12000 Angstrom thick intermetal dielectric layer composed of a low dielectric constant (1.8-3.5) polymer by spin coating on the adhesion layer;

(f) depositing a 100-2000 Angstrom thick second intermetal dielectric layer composed of a first inorganic insulator, preferably silicon nitride;

(g) depositing a 500-4000 Angstrom thick third intermetal dielectric layer composed of a second inorganic insulator, preferably silicon oxide;

(h) planarizing the third intermetal dielectric layer by chemical/mechanical polishing;

(i) depositing a photoresist layer over the third intermetal dielectric layer;

(j) exposing and developing the photoresist layer to form openings over the patterned conductive layer where via holes are required;

(k) anisotropic plasma etching the third intermetal dielectric layer in the openings in the photoresist to the second intermetal dielectric layer, using an etchant gas mixture of carbon tetrafluoride, trifluoromethane and argon;

(l) stripping the photoresist layer using an oxygen plasma while the second intermetal dielectric layer protects the first intermetal dielectric layer from oxygen damage; and

(m) anisotropically plasma etching the second and first intermetal dielectric layers to the conductive layer using the third intermetal dielectric layer as an etching mask, thereby completing via holes to the conductive layer with the first intermetal dielectric layer damage-free in the via holes, and using an etchant gas mixture containing one or more of trifluoromethane, carbon tetrafluoride and carbon dioxide with a carrier gas of argon.

USE - Manufacture of **integrated circuits** on **semiconductor** substrates, particularly **interconnections** on ultra large scale **integrated circuits** with minimum feature sizes less than 0.25 microns.

ADVANTAGE - Improved inter- and intra-level capacitance and improved reliability.

DESCRIPTION OF DRAWING(S) - The drawings show schematic cross-sectional views for the sequence of process steps for making a damage-free low-k polymer intermetal dielectric according to an embodiment of the invention.

Opening (1)
Via hole (2)
Insulating layer (12)
Conductive layer (14)
Adhesion layer (17)
Intermetal dielectric layers (16 (IMD1), 18 (IMD2), 20 (IMD3))
Photoresist layer (30)
Metal layer (32)
pp; 11 DwgNo 6,7,8/11

59/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014418357
WPI Acc No: 2002-239060/200229
Related WPI Acc No: 2001-564386; 2002-163050; 2002-178880
XRAM Acc No: C02-072003
XRPX Acc No: N02-184325
Formation of carbon-free and oxygen-free conductive layer, used as e.g. electrode of dynamic random access memory, comprises supplying precursor in oxidizing atmosphere and in the presence of organometallic catalyst
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: MARSH E P
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010055869	A1	20011227	US 98146297	A	19980903	200229 B
			US 2001923662	A	20010807	
US 6403414	B2	20020611	US 98146297	A	19980903	200244
			US 2001923662	A	20010807	

Priority Applications (No Type Date): US 98146297 A 19980903; US 2001923662 A 20010807
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010055869	A1		13	H01L-021/8242	Div ex application US 98146297
					Div ex patent US 6284655
US 6403414	B2			H01L-021/00	Div ex application US 98146297
					Div ex patent US 6284655

Abstract (Basic): US 20010055869 A1
Abstract (Basic):
NOVELTY - A carbon-free and oxygen-free conductive layer is formed by:
(a) forming a substrate having a heated surface;
(b) forming a reactor chamber having an oxidizing atmosphere;
(c) supplying a precursor to the reactor; and
(d) supplying an organometallic catalyst to the reactor.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:
(A) formation of an **integrated circuit** comprising forming a carbon-free and oxygen-free layer on a substrate assembly;
(B) formation of a capacitor (120) on a substrate comprising sequentially forming on a substrate assembly, a bottom electrode (105) which comprises a carbon-free and oxygen-free layer (75), a dielectric layer (110) and a top electrode (115); and
(C) a process for optimizing components in a conductive layer comprising forming a conductive layer, analyzing the conductive layer for component amounts, and repeating steps of forming and analyzing, where the fixed amount of the organometallic catalyst or the concentration of oxygen in the oxidizing atmosphere is varied until carbon is detected in the conductive layer.
USE - Forming a carbon-free and oxygen-free conductive layer used

as an electrode substrate, an electrode, a barrier layer, a contact layer, an **interconnect** component, and/or a bond pad of a **semiconductor** structure e.g. memory cell structure of a dynamic random access memory (claimed).

ADVANTAGE - The process provides for **semiconductor** structures of low resistivity and avoids the poisoning of dielectric layers which may reduce the effectiveness of the structures.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of the conductive layer during fabrication.

Carbon-free and oxygen-free layer (75)
Bottom electrode (105)
Dielectric layer (110)
Top electrode (115)
Capacitor (120)
pp; 13 DwgNo 3/4

59/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014098040
WPI Acc No: 2001-582254/200165
XRAM Acc No: C01-172685
XRPX Acc No: N01-433765
Copper precursor composition for e.g. chemical **vapor deposition** of **copper** layers in **semiconductor integrated circuits**, contains **copper** precursor and alkene, alkyne and/or diene
Patent Assignee: ADVANCED TECHNOLOGY MATERIALS (ADTE-N)
Inventor: BAUM T H; XU C
Number of Countries: 081 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200166347	A1	20010913	WO 2001US7232	A	20010307	200165	B
AU 200147304	A	20010917	AU 200147304	A	20010307	200204	

Priority Applications (No Type Date): US 2000522102 A 20000309
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200166347	A1	E	71	B32B-015/20	

Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

AU 200147304	A		B32B-015/20	Based on patent WO 200166347

Abstract (Basic): WO 200166347 A1
Abstract (Basic):
NOVELTY - A **copper** precursor composition comprises a **copper** precursor and an additive. The additive is alkenes, alkynes and/or dienes.
DETAILED DESCRIPTION - A **copper** precursor composition consists of **copper** precursor and additive. The additive is alkene of formula C(R3)(R4)=C(R1)(R2) (I), alkynes of formula R''-equivalent to-R' (II), and/or dienes of formula (III).
R1-R4=H, aryl, (per)fluoroaryl, 1-8C alkyl or open-chain alkyl, 1-8C (per)fluoroalkyl or 5-6C cycloalkyl;
R', R''=H, aryl, (per)fluoroaryl, 1-8C alkyl, 1-8C (per)fluoroalkyl, vinyl or 5-6C cycloalkyl;
R1-R6=H or 1-3C alkyl; and
n=0-4.
INDEPENDENT CLAIMS are also included for the following:
(1) A method of formulating the **copper** precursor composition.
(2) New complexes of formula (hfac)**Cu**(L)x, where x=1/2 or 1 and L=(I), (II) or (III).
USE - The **copper** precursor composition is used for chemical **vapor deposition** of **copper** layers in

semiconductor integrated circuits e.g. **interconnect** metallization in **semiconductor device** structures. It is also useful for forming **copper** seed layers for subsequent electroless or electrochemical plating of **copper** and other metals, for forming **copper**-containing material on a substrate, for deposition of thin-film recording head, and for circuitization of packaging components.

ADVANTAGE - The composition increases the deposition rate, improves quality of **copper** and thin-film adhesion, and reduces **copper** impurities and problems associated with **copper** precursor decomposition that may detrimentally occur during delivery and transport to the reactor.

pp; 71 DwgNo 0/6

59/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012867468
WPI Acc No: 2000-039301/200003
Related WPI Acc No: 1996-221789; 1998-018273; 1998-100229; 2000-085051; 2000-256514; 2000-664100; 2001-023075; 2001-243820; 2002-082832
XRAM Acc No: C00-010268
XRPX Acc No: N00-029617
Storage and delivery system for dispensing high-purity gas
Patent Assignee: ADVANCED TECHNOLOGY MATERIALS (ADTE-N)
Inventor: HULTQUIST S J; KIRLIN P S; MCMANUS J V; TOM G M
Number of Countries: 080 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9959701	A1	19991125	WO 99US11420	A	19990521	200003	B
AU 9941996	A	19991206	AU 9941996	A	19990521	200019	
EP 1093395	A1	20010425	EP 99925778	A	19990521	200124	
			WO 99US11420	A	19990521		
KR 2001043742	A	20010525	KR 2000713096	A	20001121	200168	
JP 2002515570	W	20020528	WO 99US11420	A	19990521	200238	
			JP 2000549358	A	19990521		

Priority Applications (No Type Date): US 9882596 A 19980521
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9959701	A1	E	58	B01D-053/04	

Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ UG ZW

AU 9941996	A		B01D-053/04	Based on patent WO 9959701
EP 1093395	A1	E	B01D-053/04	Based on patent WO 9959701

Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

KR 2001043742	A			B01D-053/04	
JP 2002515570	W		81	F17C-011/00	Based on patent WO 9959701

Abstract (Basic): WO 9959701 A1
Abstract (Basic):

NOVELTY - Sorbent-based gas storage and dispensing system comprises storage and dispensing vessel with solid-phase physical sorbent medium, a chemi- sorbent material in the storage and dispensing vessel having chemi-sorptive affinity for an impurity of a sorbate gas and a dispensing assembly in contact with storage and dispensing vessel for selectively discharging desorbed sorbate gas from vessels.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(A) a capsule for reactively sorbing an impurity gas in an environment latently susceptible to the presence of same comprises a permselective membrane wall defining an interior volume of the capsule

and a chemisorbent material reactive with the impurity gas upon permeation of the latter through the membrane and contact with the chemisorbent material;

(B) a **semiconductor** manufacturing facility including a **semiconductor** manufacturing apparatus utilizing a gas reagent whose source is coupled in gas flow communication with the **semiconductor** manufacturing apparatus;

(C) a process for supplying a reagent gas comprising providing a storage and dispensing vessel containing a solid-phase physical sorbent medium having the reagent gas physically adsorbed, optionally chemisorbing gas phase impurities of the reagent gas in the storage and dispensing vessel for gas phase removal, desorbing reagent gas from the physical sorbent medium and discharging the desorbed reagent gas from the vessel; and

(D) a process for fabricating an electronic device structure on or in a substrate comprising providing a storage and dispensing vessel with a physical sorbent medium, desorbing the fluid from the medium and dispensing the fluid from the vessel and contacting the substrate with the dispensed fluid under conditions to effectively utilize the fluid in the substrate.

USE - Sorbent-based gas storage and delivery system for dispensing high purity gas(es) may be employed in processes, such as in **semiconductor** manufacturing industry, where a reliable source of process fluid(s) is needed due to progressive increase in electronic device **integration densities** and increase wafer sizes.

ADVANTAGE - The system reduces the pressure of stored sorbate gases by providing a vessel where a gas is reversibly adsorbed on a carrier sorbent, e.g., activated carbon. The arrangement enables high purity gas dispensing from a sorbent-based gas storage and dispensing system, even with the use of inferior grades of sorbent or even in the presence of trace impurities that would mediate decomposition of the sorbate gas.

DESCRIPTION OF DRAWING(S) - The figure is a schematic representation of a storage and delivery system.

Storage and dispensing vessel (10)
Sorbent medium (17)
Gas-impermeable membrane (136)
Chemisorbent material (138)
pp; 58 DwgNo 1/8

69/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014328540
WPI Acc No: 2002-149243/200220
XRAM Acc No: C02-046454
XRPX Acc No: N02-113105
Production of isolated metallic **interconnections** in **integrated circuits** involves deposition of a second insulating layer such that voids are formed between adjacent metal zones
Patent Assignee: FRANCE TELECOM (ETFR); STMICROELECTRONICS SA (SGSA); GAYET P (GAYE-I); HAOND M (HAON-I); TORRES J (TORR-I)
Inventor: GAYET P; HAOND M; TORRES J
Number of Countries: 027 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1111669	A1	20010627	EP 2000410161	A	20001222	200220 B
US 20010036723	A1	20011101	US 2000742891	A	20001220	200220
FR 2803092	A1	20010629	FR 9916488	A	19991224	200220

Priority Applications (No Type Date): FR 9916488 A 19991224
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1111669	A1	F	9	H01L-021/768	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR				
US 20010036723	A1			H01L-021/4763	
FR 2803092	A1			H01L-021/28	

Abstract (Basic): EP 1111669 A1
Abstract (Basic):
NOVELTY - Circuit metallization level formation comprises forming metal zones (11-14) laterally separated by a first insulating layer, removing the latter using a mask, to leave protection zones (21) around metal zone parts to be contacted by a via passing through a second insulating layer (24), and depositing the second insulating layer (24) such that voids are formed between adjacent metal zones.

DETAILED DESCRIPTION - The metal zones (11-14) are made of **copper**, silver or gold or various alloys **copper** with materials selected from **aluminum**, silicon, manganese and cobalt.

The second insulating layer (24) deposited non-conformally such that gaps are formed between adjacent metal zones is of a material selected from silicon oxide and silicon oxides doped with fluorine and/or carbon, and is deposited by chemical **vapor deposition**.

The second insulating layer (24) can also be a porous layer of an aerogel or a xerogel.

USE - **Integrated semiconductor circuit** production.

ADVANTAGE - Reduced parasitic capacitance between metallization portions at the same level is obtained by using a second insulating layer having voids between adjacent metallic portions, or made of a

porous material.

DESCRIPTION OF DRAWING(S) - The drawing shows a final stage in the formation of **interconnections** by a process according to the invention.

Metal zones (11-14)
Protection zones (21)
Second insulating layer (24)
pp; 9 DwgNo 4/8

69/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014050794
WPI Acc No: 2001-535007/200159
XRAM Acc No: C01-159290
XRPX Acc No: N01-397183
Fabrication of dual damascene structures useful in, e.g., **integrated circuit** microelectronic fabrications, involves employing spin-on polymer etch stop layer
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: JANG S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6265319	B1	20010724	US 99387440	A	19990901	200159	B

Priority Applications (No Type Date): US 99387440 A 19990901
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6265319	B1		13	H01L-021/00	

Abstract (Basic): US 6265319 B1
Abstract (Basic):
NOVELTY - A dual damascene structure is fabricated by employing spin-on polymer etch stop layer.
DETAILED DESCRIPTION - Formation of a dual damascene structure comprises (a) forming a first dielectric layer (14') over a substrate (10) having contact regions (12a-c); (b) forming an intermediate carbon-containing low dielectric constant dielectric layer (16'), upon the first dielectric layer; (c) forming a second dielectric layer (18'), upon the intermediate dielectric layer; (d) forming a first patterned photoresist etching mask layer which defined contact via holes, over the second dielectric layer; (e) etching through the first patterned photoresist mask layer employing a first anisotropic reactive etch process, and transferring the pattern into and through the second dielectric layer, intermediate dielectric constant dielectric layer, and first dielectric layer; (f) stripping the first patterned photoresist etch mask layer; (g) forming a second patterned photoresist etch mask layer defining a trench pattern, over the substrate; (h) etching through the second patterned photoresist etch mask layer employing a second anisotropic reactive etch process, and transferring the trench pattern into the second dielectric layer, using the intermediate dielectric layer as an etch stop layer, thus forming an etched contact via hole and trench pattern; and (i) striping the second patterned photoresist etch mask layer.
USE - For forming dual damascene structures, i.e., metal **interconnection** layers useful in microelectronic fabrications, such as, **integrated circuit** microelectronic fabrications, charge coupled device microelectronic fabrications, light emitting diode microelectronic fabrications, and flat panel display microelectronic fabrications (claimed).

ADVANTAGE - The invention provides a dual damascene stacked conductor **interconnection** layer with reduced inter-level capacitance and lowered electrical resistance.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional schematic view of the dual damascene structure.

Substrate (10)
Contact regions (12a-c)
First dielectric layer (14')
Intermediate dielectric layer (16')
Second dielectric layer (18')
Conductor material (28)
Dual damascene **interconnection** layer (29)
pp; 13 DwgNo 4/12

69/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013796525
WPI Acc No: 2001-280736/200129
XRAM Acc No: C01-085177
XRPX Acc No: N01-200135
Manufacture of **semiconductor device** involves forming metal layer over surface of **semiconductor** wafer substrate in ohmic contact with features of underlying in-laid metallization pattern
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: BUYNOSKI M S; LIN M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6207553	B1	20010327	US 99237258	A	19990126	200129	B

Priority Applications (No Type Date): US 99237258 A 19990126
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6207553	B1		10	H01L-021/4763	

Abstract (Basic): US 6207553 B1
Abstract (Basic):
NOVELTY - A **semiconductor device** is made by forming a metal layer over a surface of a **semiconductor** wafer substrate in ohmic contact with features of an underlying in-laid metallization pattern; and patterning the metal layer by a selective anisotropic etching process where an exposure mask having predetermined openings is placed over the metal layer in spaced relation with the metallization pattern.

DETAILED DESCRIPTION - Manufacture of a **semiconductor device** includes providing a substrate comprising a **semiconductor** wafer with a surface having a dielectric layer. The dielectric layer comprises a surface including a first in-laid metallization pattern. The pattern includes spaced-apart metal features forming electrical contacts, vias, interlevel metallization, and/or **interconnect** routing of at least one active device region or component of the wafer substrate. A preselected metal layer is formed to a predetermined thickness over the surface of the dielectric layer and in ohmic contact with each of the metal features of the first in-laid metallization pattern. The metal layer includes a surface. A patterned exposure mask is positioned at a predetermined spacing from the surface of the metal layer. The mask comprises a predetermined pattern of openings. The mask openings are positioned in a predetermined registered relation with the features of the first in-laid metallization pattern. A gas atmosphere is established in the space between the surface of the metal layer and the patterned exposure mask. It comprises etchant material(s) for photo-activated anisotropic etching of the metal layer. The portions of the gas atmosphere exposed through the pattern of mask openings are irradiated with radiation of predetermined wavelength(s) for effecting photo-activated, selective,

anisotropic etching of the portion of the metal layer exposed through the pattern of mask openings. The photo-activated selective anisotropic etching step is continued for an interval to remove the entire thickness of the metal layer at the exposed portions, thus forming a patterned metal layer having predetermined portions in overlying ohmic contact with selected features of the first in-laid metallization pattern.

USE - The inventive method is used for manufacturing a **semiconductor device**. It is applicable to the formation of various types of submicron-dimensioned metallization patterns, including, but not limited to, high aspect ratio in-laid metallization patterns employed in back-end processing of **integrated circuit semiconductor devices**.

ADVANTAGE - The invention enables rapid formation of reliable, defect-free, in-laid, multi-level back-end contacts and **interconnections**. It also effects an increase in manufacturing throughput by reducing the time and cost of conventional metal layer patterning vis-a-vis conventional methodology employing photolithographic masking and etching techniques. It increases product reliability and yield.

DESCRIPTION OF DRAWING(S) - The figure illustrates a simplified, cross-sectional form of a portion of a multi-metallization layer back-end contact/**interconnect** structure of an **integrated circuit semiconductor device**.

pp; 10 DwgNo 1/3

69/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013522828
WPI Acc No: 2001-007034/200101
XRAM Acc No: C01-001707
XRPX Acc No: N01-005055

Deposition of a material in substrate formation involves allowing deposition of material in a formation of the substrate and suppressing deposition of the material at the substrate surface plane

Patent Assignee: CVC PROD INC (CVCC-N)
Inventor: MOSLEHI M M

Number of Countries: 092 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200063966	A2	20001026	WO 2000US8676	A	20000330	200101	B
AU 200040610	A	20001102	AU 200040610	A	20000330	200107	
US 6245655	B1	20010612	US 99285162	A	19990401	200135	

Priority Applications (No Type Date): US 99285162 A 19990401
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200063966	A2	E	43	H01L-021/768	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW

AU 200040610	A		H01L-021/768	Based on patent WO 200063966
US 6245655	B1		H01L-021/44	

Abstract (Basic): WO 200063966 A2
Abstract (Basic):

NOVELTY - A material is deposited in a substrate formation by exposing the substrate (12) to a process gas (24) for depositing the material, suppressing deposition of the material on the substrate surface plane (22), and ceasing deposition of the material when the material fills the formation (18) to the substrate surface plane.

USE - For deposition of a material useful in fabrication of an electronic device, e.g. **semiconductor integrated circuit** chip.

ADVANTAGE - The invention forms inlaid structures with minimal or no need for chemical-mechanical polishing of the substrate surface after deposition of the material. It has minimal wafer handling, wafer process time, and waste product generation. Reduced material nucleation and deposition along the sidewalls (28) of the formation allows void-free filling of material in the formation with larger grain size and improved metallization reliability. It is compatible with integration of various low k dielectrics and with free-space dielectrics. It allows direct interlevel **copper**-to-**copper** contacts between **interconnect** plugs and lines without the use of

diffusion barrier, resulting in improved **interconnects** performance and reduces chip production costs.

DESCRIPTION OF DRAWING(S) - The figure shows a side cutaway view of inlaid line formations in a substrate having material deposition.

Substrate (12)
Formation (18)
Surface plane (22)
Process gas (24)
Bottom surface (26)
Sidewall(30) Enhancement agent (28)
Blocking agent (32)
Adhesion layer (34)
pp; 43 DwgNo 3A/6

69/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012814634
WPI Acc No: 1999-620865/199953
XRAM Acc No: C99-181338
XRPX Acc No: N99-457921
Fabricating **semiconductor integrated circuit** chip structures for microprocessors and digital signal processors
Patent Assignee: CVC PROD INC (CVCC-N); CVC INC (CVCC-N)
Inventor: MOSLEHI M; MOSLEHI M M
Number of Countries: 021 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9954934	A1	19991028	WO 99US8475	A	19990422	199953	B
US 6016000	A	20000118	US 9864431	A	19980422	200011	
EP 1000440	A1	20000517	EP 99917606	A	19990422	200028	
			WO 99US8475	A	19990422		
US 6124198	A	20000926	US 9864431	A	19980422	200051	
			US 98187297	A	19981105		
KR 2001020476	A	20010315	KR 99712124	A	19991222	200159	
JP 2002506577	W	20020226	JP 99553180	A	19990422	200219	
			WO 99US8475	A	19990422		

Priority Applications (No Type Date): US 98187297 A 19981105; US 9864431 A 19980422
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9954934	A1	E	78	H01L-023/48	
Designated States (National): JP KR					
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
US 6016000	A			H01L-029/00	
EP 1000440	A1	E		H01L-023/48	Based on patent WO 9954934
Designated States (Regional): DE FR GB IT NL					
US 6124198	A			H01L-021/768	Div ex application US 9864431 Div ex patent US 6016000
KR 2001020476	A			H01L-023/48	
JP 2002506577	W		54	H01L-021/768	Based on patent WO 9954934

Abstract (Basic): WO 9954934 A1
Abstract (Basic):
NOVELTY - An ultra-high-speed multilevel chip **interconnect** structure using a free-space dielectric medium is provided for a **semiconductor integrated circuit** (**IC**) chip.
DETAILED DESCRIPTION - A multilevel **interconnect** structure for a **semiconductor IC** chip for a **semiconductor** substrate comprises:
(a) electrically conductive metallization levels with **interconnect** segments;
(b) plugs for connecting various metallization levels and the **semiconductor devices**;
(c) a free-space medium occupying at least a portion of the

electrically insulating regions within the multilevel **interconnect** structure; and

(d) an electrically insulating top passivation overlayer for hermetic sealing and for protection of the **IC** chip, which also serves as a heat transfer medium for facilitating heat removal from the **interconnect** structure and provides mechanical support for **interconnect** structure through contact with the top metallization level of the multilevel **interconnect** structure.

An INDEPENDENT CLAIM is also included for a method for the fabrication of a multilevel **interconnect** structure.

USE - The method is used for the fabrication of **semiconductor IC** chips to be use in microprocessors and digital signal processors (DSP).

ADVANTAGE - The invention offers improved **interconnect** structures and methods which will reduce the parasitic effects and enhance the **semiconductor integrated circuit** speed and operational reliability. Simplification at the **interconnect** process is enabled and chip manufacturing cost is reduced. The invention provides the use of a free-space interlevel/intermetal dielectric (ILD/IMD) medium. It is compatible with damascene (single /dual) **interconnect** fabrication process with a reduced number of process steps per **interconnect** by four steps. Its compatibility is applicable to various types of **interconnect** metallization materials such as **copper**, gold, silver, **aluminum**, and other superconducting materials. It provides excellent thermal management and efficient heat dissipation removal capabilities. The **interconnect** structure provides reduce RC propagation delay and reduced capacitive crosstalk. **Interconnect** metallization electromigration lifetime is improved. It neglects the use of low-k dielectric materials, relatively complex and expensive process integration methods. The invention provides hermetic sealing of the multilevel **interconnect** structure and **semiconductor IC devices**. It also provides excellent mechanical strength and integrity of the multilevel **interconnect** structure and overall **semiconductor** chip (claimed).

DESCRIPTION OF DRAWING(S) - The drawing shows a multilevel **interconnect** structure following formation of an etchant-transmission window pattern on the top layer and after formation of a free-space dielectric medium.

pp; 78 DwgNo 13/15

69/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012784757
WPI Acc No: 1999-590983/199950
Related WPI Acc No: 1998-110891; 1998-110893; 1999-255032; 1999-255117; 1999-255227; 1999-468688; 1999-551265; 1999-551266; 2000-039212; 2000-039214; 2000-147588; 2000-638564; 2000-665147; 2001-521767; 2002-188187; 2002-240711; 2002-370617
XRAM Acc No: C99-172499
XRPX Acc No: N99-435934
Electrolytic deposition of **copper** layer
Patent Assignee: SEMITOOL INC (SEMI-N); CHEN L (CHEN-I); MCHUGH P R (MCHU-I); RITZDORF T L (RITZ-I); WEAVER R A (WEAV-I); WILSON G J (WILS-I)
Inventor: CHEN L; MCHUGH P R; RITZDORF T L; WEAVER R A; WILSON G J
Number of Countries: 024 Number of Patents: 010
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9947731	A1	19990923	WO 99US6306	A	19990322	199950	B
EP 1064417	A1	20010103	EP 99912827	A	19990322	200102	
			WO 99US6306	A	19990322		
US 6197181	B1	20010306	US 9845245	A	19980320	200115	
CN 1293719	A	20010502	CN 99804128	A	19990322	200143	
US 6277263	B1	20010821	US 9845245	A	19980320	200150	
			US 9885675	P	19980515		
			WO 99US6306	A	19990322		
			US 99387099	A	19990831		
US 6290833	B1	20010918	US 9845245	A	19980320	200157	
			US 9885675	P	19980515		
			WO 99US6306	A	19990322		
			US 99387033	A	19990831		

Priority Applications (No Type Date): US 9885675 P 19980515; US 9845245 A 19980320; US 99387099 A 19990831; US 99387033 A 19990831; US 2001885232 A 20010620; US 99129055 P 19990413; US 99143769 P 19990712; US 2000182160 P 20000214; WO 2000US10120 A 20000413; US 2000206663 P 20000524; US 2000732513 A 20001207

Abstract (Basic): WO 9947731 A1
Abstract (Basic):
NOVELTY - The electroplating bath contains **copper** sulfate, ammonium sulfate, a complexing agent and ethylene glycol.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:
(a) applying a metallization **interconnect** structure to a workpiece by **PVD** of an ultrathin metal seed layer 50-500 Angstrom thick, then enhancing this seed layer by electrodepositing a **copper** layer using the above plating bath, giving a total thickness on sidewalls of recessed features at least 10% that of the layer thickness on the exterior of the workpiece;
(b) a method as in (a) except that the workpiece contains a barrier layer; and
(c) the apparatus used.

USE - Application of a **copper** metallization **interconnect** structure to an **integrated circuit**.

ADVANTAGE - The conformal **copper** layer is deposited with good uniformity, even in the trenches, vias and other microstructures. The **copper** layer has lower resistivity than **aluminum** layers, thus allowing higher performance **integrated circuits** to be fabricated.

DESCRIPTION OF DRAWING(S) - The drawing shows a schematic view of the apparatus used.

semiconductor wafer as cathode (30)
anode (35)
plating solution (50)
diffuser (55)
pp; 55 DwgNo 3/7